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FPGA implementation of a digital signal component separator and a disturbance compensator for the LANSCE 805 MHz solid-state high power RF amplifier

Monday 11 August 2025 16:00 (2 hours)

Because of aging, and product discontinuity, LANSCE is investigating the replacement of high power RF amplifiers. A promising candidate is the GaN solid-state power amplifier (SSPA). For a high drain voltage, the drain power dissipation of SSPA is increased as the operating efficiency becomes low. The outphasing technique provides high efficiency operation of the SSPA. The outphasing amplifier converts one Amplitude Modulation-Phase Modulation(AM-PM) signal to two PM only signals by the signal component separator(SCS), and these PM only signals are amplified by amplifiers linearly. The combination of the amplified PM only signals yields the linear amplification of the AM-PM input signal.
In this paper, a digital SCS (DSCS) in In-phase/Quadrature(I/Q) coordinate is proposed. The DSCS is implemented on the Field Programmable Gate Array(FPGA) based LANSCE digital low level RF (DLLRF) control system. In addition, a digital disturbance observer based compensator is implemented to detect and suppress the amplitude and phase disturbances existing on the RF forward paths. The performances of the DSCS and the disturbance compensator are verified on a low power testbench.

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No

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No

Footnotes

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Yes

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