DESIGN AND TESTING OF A UNIVERSAL EMBEDDED FEEDBACK CONTROLLER FOR RF CAVITIES

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Abstract

The design of Low-Level Radio Frequency (LLRF) controllers used to stabilize the amplitude and phase of the field within the RF cavities is typically customized to the frequency and mode of operation. IUAC, New Delhi, India, operates accelerators with RF structures in the range of 12.125-97 MHz, in both normal and superconducting modes. Currently, all the LLRF controllers are structure-specific and designed in the analog electronics domain. Component aging and obsolescence have made it challenging to maintain them due to frequent failures. To overcome this, a universal digital controller has been developed whose design is based on the philosophy of using the same hardware for all the RF structures at IUAC. It is a compact, frequency-reconfigurable, standalone device controlled by an EPICS IOC. With an aim to cater to the requirements of multi-accelerator facilities, this controller has been tested as a Sawtooth Waveform Generator for the Multi-Harmonic Buncher (MHB), as a generator-driven (GDR), and as a self-excited loop (SEL)-based LLRF for various RF cavities at IUAC. Long-term RMS stability of ~1% in amplitude and a $< \pm 0.4^\circ$ in phase locks have been obtained. Design details and test results are discussed in this paper.

INTRODUCTION

RF resonant cavities are the heart of an RF accelerator, which energizes incoming ion beams. These structures use extremely high axial electric fields inside them and transfer their energy to the incoming beam particles. For effective energy transfer, the stability of this field, in terms of amplitude and phase, is paramount. This stability is achieved using the LLRF controllers. A small fraction of the cavity field is picked up and fed into this controller as feedback, which then performs feedback control algorithms to ensure the required stability. At IUAC, there are multiple RF structures, including the Superconducting Linear Accelerator (SC-LINAC), the High Current Injector (HCI), a Multi-Harmonic Buncher (MHB) for the Pelletron DC Accelerator, and a Table-Top (TT) Cyclotron. The operating frequency of RF cavities ranges from 12.125 MHz to 97 MHz. The LLRF electronics for all these RF structures are in the analog domain and have been in use for many years [1–3]. The SC-LINAC has SEL-based LLRF [2, 4, 5], whereas HCI, MHB, and TT cyclotron use GDR-based electronics [1, 3]. While the current solutions have performed satisfactorily, maintenance cycles have recently grown due to component-level issues. These controllers are rigid in their designs with limited modification capabilities. Maintaining spares inventory is also a challenging task amid component obsolescence. Analog techniques used for cavity field stabilization were first proposed in [4, 5]. Since then, many advancements, especially the introduction of high-speed A/D and D/A converters and specialized signal-processing hardware, have led to the widespread development of digital LLRF electronics [6–11]. Several implementations invoke backplane-based methods, such as VME, cPCI, and microTCA. These solutions are often costly, bulky, and difficult to adopt due to a customized design goal. Standalone, non-crate-based systems provide a more versatile, fast, and cost-effective alternative. The use of a SoC-FPGA makes this a complete system implementation, as the same chip can host both the signal-processing logic and the remote-control server logic. This paper builds-up from the findings of [10, 11] to devise an universal digital LLRF design that can be used as a sawtooth waveform generator for MHB, GDR-based RF controller for HCI, and TT cyclotron, and SEL-based RF controller for SC-LINAC. The main feature of our design is the hardware configuration, which remains the same regardless of the cavity type, without the need for FPGA reprogramming. In addition to the LLRF algorithm, the same FPGA contains logic for the motorized Frequency Tuner Control, considerably lowering the system's cost. Besides that, a set of EPICS device drivers has also been written for generic record types (AI, AO, BI, BO, MBBI, MBBO) in the processor part of the System-on-Chip Field Programmable Gate Array (SoC-FPGA) [12]. EPICS Qt-based code-free GUI is used for remote control. Further sections detail its construction and test results with various facilities at IUAC.

DESIGN AND CONSTRUCTION

The major blocks of the system as shown in the overall physical block diagram (Fig. 1a) are a wideband Analog Front-End (AFE), microcontroller programmed PLL Multiplier, and a SoC-FPGA-based digital board. Different blocks of the finished prototype (Fig. 1b) are explained in the following subsections.

Analog Front–End (AFE)

This module (Fig. 2) is responsible for the down- and up-conversion of RF signals entering or leaving the digital board. Since the design philosophy is universal, it features wideband components to convert all incoming RF signals

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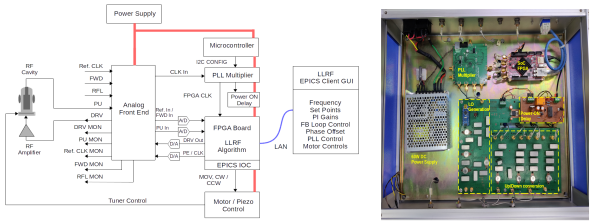

(a) (b)

Figure 1: Block Diagram (a) and Finished Prototype (b) of the Universal LLRF System.

to the low-frequency domain and vice versa. In addition, it also provides various signals for monitoring purposes. It is essentially a combination of attenuators, amplifiers, mixers, low- and high-pass filters, and directional couplers. The local oscillator signal for the mixer is generated by a Si5356-based I2C-programmable PLL multiplier, synchronized with an external reference signal. Apart from the LO signal, it is used to generate a 125 MHz system clock signal for the FPGA. An on-board microcontroller loads a frequency-control configuration into the PLL multiplier at power-up, so that all signals are stabilized before the system actually powers up.

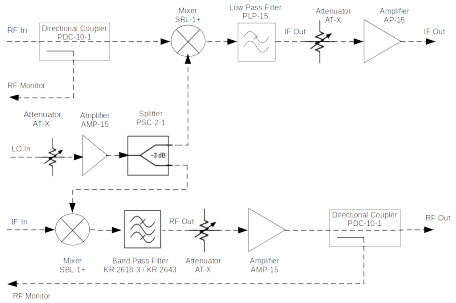

Figure 2: Block Diagram of the Analog Front End Module.

Digital Board

This board [13] houses the main signal processing algorithm. An on-board fast ADC samples the downconverted RF input signal and passes it through the algorithm (Fig. 3). Our controller can operate in multiple modes, as listed below, with suitable support from an EPICS IOC-based control server. A lightweight digital PLL (DPLL) forms an important aspect shown at the bottom of the algorithm (Fig. 3) It helps the Si5356-based PLL multiplier mitigate long-term sub-millihertz-level errors which were experimentally observed and caused by accuracy issues with the manual setting of its phase increment word via the GUI. It is lightweight since the incoming signal has only two levels (low and high), so no explicit multiplications are needed—only sign inversions of the local oscillator—followed by a very sparse 23-tap FIR filter and a slow integrator.

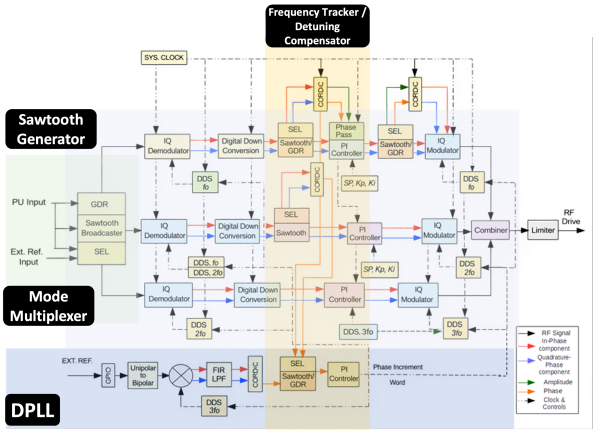

Figure 3: Digital Feedback Control Algorithm for Universal LLRF.

Sawtooth Generator: In this mode, the system is programmed to host three similar LLRF digital signal processing chains. Each chain independently stabilizes the phase and amplitude of a particular harmonic frequency as detailed in [11]. It is used to drive multiple LC-tank circuits at the MHB of Pelletron [1] and HCI [3] facilities of IUAC.

Generator Driven Resonator (GDR): In this mode, the system is used to regulate a single frequency RF cavity field based on an external master–oscillator signal. This algorithm operates in the IQ domain and uses a single signal processing chain from the multiple available on the FPGA. Direct control of any frequency signal up to 50 MHz is possible, and beyond that, the AFE is used to downconvert the signal. These controllers are helpful in the HCI and tested with TT cyclotron project of IUAC [9]. In addition to the cavity field feedback control, this mode also features a PWM-controlled motorized frequency tuner in the same FPGA as per [10]. It compares the phase error (between the forward signal and the pick-up signal) with a threshold value and, based on that, it decides the direction of motion of the tuner [9, 10].

Self-Excited Loop (SEL): In this mode, the system is programmed to excite an oscillation in a Superconducting RF cavity at its natural frequency [8]. The concept of SEL has been practically implemented in the analog domain in [2, 4, 5]. The present design is inspired by [7, 8] and implemented in the digital domain using the Phase-Pass method. Here, the CORDIC algorithm is used to convert from the IQ domain to the amplitude/phase domain, enabling the amplitude limiter and phase shifter to be digitally implemented via simple mathematical operations. In the case of free-running SEL, the DPLL helps to lock the on-board DDS clock with the pick-up signal. However, in the case of external signal based amplitude and phase locking in the SEL mode (SEL-AP), the same DPLL can lock the DDS clock to an external reference. Once the DDS is locked, the Amplitude/Phase PI controller takes over to stabilize the pick-up signal. This relationship,

shown in the algorithm (Fig. 3), is easily navigated using the suitable options in the GUI.

Remote Control and Firmware

The SoC-FPGA hosts a remote-control server which is a layered, multi-tier architecture (Fig. 4) based on Ethernet PHY. All the modes of operation are programmed into a single, Xilinx Zynq-based SoC-FPGA board [13]. Navigating and controlling them in remote is done through software-programmable, memory-mapped, Advance eXtnesible Interface (AXI)-controlled General Purpose IO (GPIO) variables. All analog control parameters, such as set points, PI gains, and phase-shift values, are passed via multi-bit AXI GPIOs. A specialized set of generic EPICS [14] device drivers has been written to perform different types of input/output transactions [12]. Entire backend computations are optimally performed in the IOC using various types of EPICS records, leading to a simplified EPICS Qt-based code-free GUI.

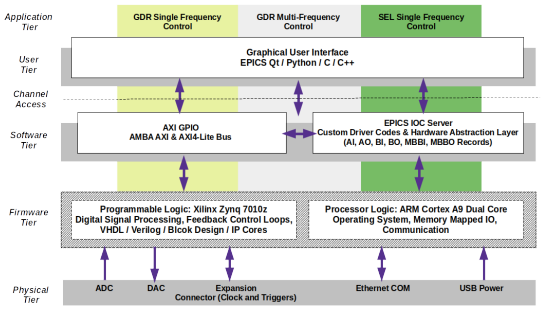

Figure 4: Firmware Architecture.

TESTS AND RESULTS

Three prototype units bearing the same hardware have been deployed with the MHB of the Pelletron Beam Pulsing System (BPS), TT cyclotron, and the Superconducting Test Cryostat (STC) of the SC–LINAC facilities at IUAC, New Delhi. The MHB operates under direct RF sampling with three harmonics of f_o = 12.125 MHz, whereas for TT cyclotron, the operational frequency is 18.2 MHz. Lastly, the NCRF cavities at the HCI facility are operational at 48.5 MHz and 97 MHz, serving as the injector for the SC-LINAC, with several Quarter Wave Resonators (QWRs) operating at 97 MHz. The signals for these controllers were first down-converted and then fed to the digital board for direct RF sampling. The controller has been tested with a chopped $^{28}Si^{6+}$ beam of 80–100 MeV at the MHB-BPS of IUAC, where it produced a stable pulsed beam with 1.5–1.8 ns FWHM for nuclear physics experiments. This performance is on par with the existing analog-domain controller. For the TT–cyclotron (Fig. 5a), this controller in GDR mode has been operated with a frequency tuner up to 200W RF power. In the STC test, the SEL mode could successfully strike the loop at the cavity's resonance, and the DPLL was found to track it up to a few hundred hertz in the room-temperature SEL test (Fig. 5b), affected by coupler movement and underlying microphonics. In the laboratory environment, the long–term RMS stability (Fig. 6) of the controller was also recorded across various modes of operation.

(a) (b)

Figure 5: Test setup of TT Cyclotron (a) and SCRF Cavity at room-temperature (b).

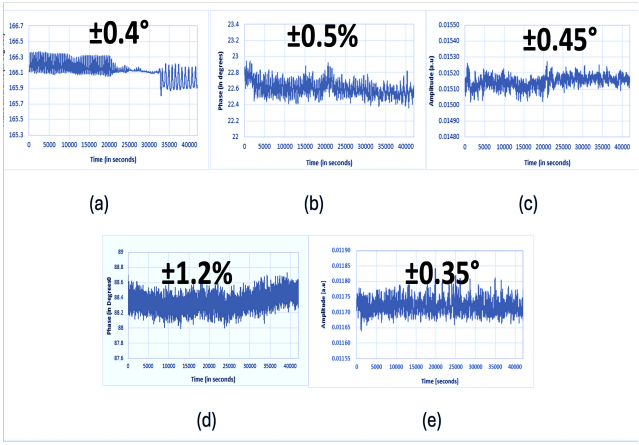

Figure 6: Long–Term RMS Variations in (a) Phase of MHB-DPLL, (b) Amplitude, and (c) Phase in GDR mode, and (d) Amplitude, and (e) Phase in SEL-AP mode of Operation of the Universal LLRF.

CONCLUSION

This paper successfully demonstrates the concept, design, and implementation of a universal LLRF controller. It is a compact, stand-alone instrument featuring advanced signal processing and novel frequency-tracking algorithms implemented on a single FPGA board. This controller is suitable for any multi-accelerator facility, such as IUAC in New Delhi. Phase and Amplitude locks were stabilized in the range of ~0.4° and ~1% respectively. Control loop's dynamic range extends up to 35° in phase and ±3 dB in amplitude corrections, verified using an additional phase shifter and attenuator. After rigorous testing at IUAC, this controller will undergo mass production for beam acceleration.

ACKNOWLEDGEMENTS

The authors sincerely thank Prof. A.C. Pandey, Director of IUAC, New Delhi, for inspiring this collaborative research, and are grateful for the support received from the SENSe and BSTTM Departments at IIT Delhi.

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