THE MYRRHA PHASE 1 MTCA.4-BASED LLRF SYSTEM

A. Bellandi, W. De Cock, F. Frank, J. Geerts, K. Geerts, E. Verhagen,
Belgian Nuclear Research Centre, Mol, Belgium

Abstract

The first 100 MeV stage of the MYRRHA superconducting RF linear accelerator is under construction in Mol, Belgium. The machine will produce an instantaneous proton beam current of 4 mA and represents the first step toward the construction of the MYRRHA Accelerator-Driven System (ADS). Such a machine presents several technical challenges for the control of its RF cavities. First, the required field stability is $\leq 0.1\%$ in amplitude and $\leq 0.1^\circ$ in phase to avoid excessive beam losses. The high loaded quality factor ($Q_L = 2.3 \times 10^6$) and the need to modulate the beam at 250 Hz require sophisticated field- and detuning-control techniques to keep RF power consumption and stability within specifications. Finally, since the maximum allowed beam-trip duration is less than 3 s, real-time fault detection and recovery techniques must be implemented in the Low-Level RF (LLRF) controller. To meet these stringent requirements, the MTCA.4 standard and the RFSoC-based DAMC-DS5014DR direct-sampling AMC were chosen. In this proceeding, the LLRF control strategy foreseen for MYRRHA Phase 1 will be presented. The current status of the firmware, software, and analog front-end will also be discussed.

INTRODUCTION

MYRRHA Phase 1 [1] aims to demonstrate the reliability and flexibility required to build an Accelerator-Driven System (ADS). The core of the project is a 4 mA, 70 MeV Continuous-Wave (CW) superconducting proton LINAC, with the option to later extend it to 100 MeV (Fig. 1). Apart from reliability studies, the facility features the Proton Facility (PTF) and Full Power Facility (FPF) to perform nuclear and solid-state physics studies, R&D for fourth-generation nuclear power plants and fusion reactors and enable the production of theranostic radioisotopes. The first part of the accelerator is a 16.6 MeV normal-conducting injector with resonators operating at 176 MHz.

The second part of the accelerator is a superconducting LINAC. The cavities chosen for this section are single-spoke cavities operating at 352.2 MHz. In total, up to 80 resonators will be installed in this phase of the project (see Table 1). The construction of this machine poses unique challenges to the accelerator community: first, the infrastructure targets 40 years of operations. In addition, it requires mean time between failure values at the same level as nuclear power installations. Finally, contrary to most large-scale high-energy particle accelerators in operation today, MYRRHA Phase 1 is designed to operate with continuously varying beam duty factor. To reach these requirements, the Low-Level Radio Frequency (LLRF) control system plays a crucial role. This paper therefore focuses on the implementation status of the proposed LLRF architecture and on the main functions currently under development and integration. To minimize the risks, MYRRHA's ACcelerator Electronics (ACE) group is currently collaborating with Deutsches Elektronen-Synchrotron (DESY). Not only the field controller card, the DAMC-DS5014DR [2], is currently being designed by DESY, but it is planned to reuse several of their firmware and software packages that are currently deployed in high-reliability superconducting LINACs [3, 4]. Despite the collaboration, several components, such as resonance control, statistics collection, deterministic system reconfiguration, fault detection, post mortem data acquisition, and beam loading compensation techniques, still need to be implemented and integrated to address the unique requirements of MYRRHA.

HARDWARE

The hardware platform chosen for the LLRF system is based on the MicroTCA.4 (MTCA.4) standard. The motivation to choose this crate form factor is to achieve high reliability, redundancy and modularity. Each crate will have up to 4 DAMC-DS5014DR boards to drive an equivalent number of cavities. The synchronization of the boards is orchestrated by a single White Rabbit-capable Advanced Mezzanine Card (AMC) that is interfaced with the DAMC-DS5014DRs through the MTCA.4 backplane. The timing board is responsible for generating machine triggers and communicate beam parameters and machine configuration data to the controller in real-time. A CPU AMC, communicating with the RF boards using the PCI express bus of the MTCA.4 crate provides, if needed, additional computing and diagnostic capabilities to the LLRF system.

DAMC-DS5014DR

DAMC-DS5014DR is an RFSoC-based AMC that is optimized for RF-based applications. The board is chosen for several reasons: The use of direct sampling allows using the board for the accelerator frequencies and, possibly, for future 704.4 MHz elliptical cavities foreseen in MYRRHA phase 2. Additionally, using direct sampling simplifies the analog front-end electronics by eliminating the need of additional RF mixers. The ADCs and DACs of the board are driven at 4930.8 MSps and the measured signals are digitally downconverted using a numerically controlled oscillator. Then the signals are decimated to 12.327 MSps. The clock frequency of the programmable logic is 123.27 MHz. Apart from the RF converters and programmable logic, the board also features a quad core ARM A53 processor and two ARM Cortex R5 realtime processors. The A53 processor runs the main LLRF EPICS Input-Output Controller (IOC) on embedded Linux. This IOC directly communicates with the System-on-Chip (SoC) programmable logic. The cus-

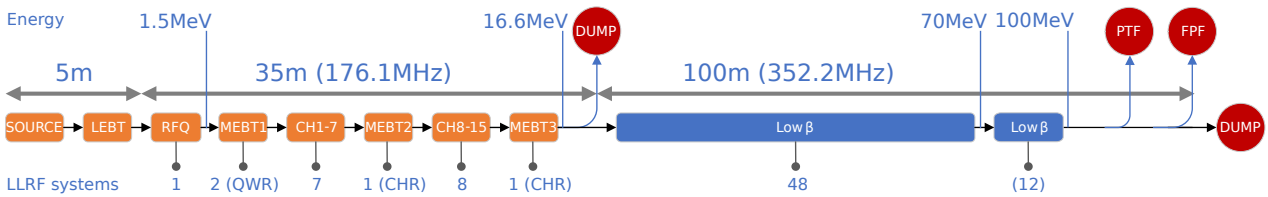

Figure 1: Layout of the MYRRHA Phase 1 accelerator highlighting LLRF systems. Two CH cavities are installed in the Medium Energy Beam Transfer (MEBT) lines for rebunching purpouses (CHR).

Table 1: Main RF parameters of the accelerating cavities. Numbers in parentheses indicate the total cavities for the full MYRRHA Phase 1 100 MeV configuration.

Cavity	**Qty.**	f_0 (MHz)	β	Q_L	$f_{1/2}$ (Hz)	r/Q (Ω)	$E_{\mathrm{acc,max}}$ (MV/m)
RFQ	1	176.1	0.0080-0.056	2.0×10^3	4.4×10^4	73	0.37
QWR	2	176.1	0.0569	5.3×10^3–5.7×10^3	1.3×10^4–1.5×10^4	385.4	1.6
CH	17	176.1	0.058–0.183	5.3×10^3–8.5×10^3	1.0×10^4–1.7×10^4	584–4569	1.8
Spoke	48 (60)	352.2	0.351	2.3×10^6	7.6×10^1	200.8	9.1

tom Real Transition Module (RTM) design in development for MYRRHA, paired with the DAMC-DS5014DR via the MTCA.4 zone-3 connector, provides all the analog signal conditioning features, like programmable amplification, attenuation, gating, and power protection required to match the specifications of the RFSoC's converters. The RTM also applies low-pass filtering with a 1.5 GHz bandwidth thus enabling the use of this RTM for MYRRHA for all the resonance frequencies of Phase 1 and Phase 2 cavities.

Piezoelectric Driver

The superconducting spoke cavities are designed to have a half bandwidth of 76.6 Hz. Since the expected Lorentz Force Detuning (LFD) coefficient is around 7 Hz/(MV/m)^2, driving the resonators at gradients higher than 4 MV m^{-1} triggers the ponderomotive instability regime [5]. In addition, cryogenic fluid pressure variations and microphonics require active compensation to minimize the power expenditures. Finally, in case of a station fault, the affected cavity should be detuned by several cavity bandwidths in less than 3 s to minimize beam generation downtime. Therefore, piezoelectric tune control is implemented for these cavities. The piezoelectric elements have a capacitance of 4 µF at cryogenic temperatures and are operated between −40 V and 160 V. The piezoelectric tuner system has a DC sensitivity of 10 Hz V^{-1} [6] and it is expected that the driver will be able to drive it with a resolution of at least 25 mV. The driver of the piezoelectric tuners is going to be installed in a 19" rack enclosure and will be able to receive commands from the RF AMC, with sample rates up to 30 kHz, using a dedicated low-latency optical uplink. The driver will also continuously monitor the driving current and voltage and send this information to the MTCA.4 RF card for monitoring purposes.

LLRF FIRMWARE AND SOFTWARE MODULES

The LLRF of MYRRHA is being developed following a modular approach (Fig. 2). The main functions targeted in the current implementation are listed below.

Field Control A digital feedback loop block is being implemented to compensate model uncertainties and disturbances. Two operating modes are available: Generator-Driven Resonator (GDR) mode for normal operation with beam and Self-Excited Loop (SEL) mode for system characterization and testing. The internal signals are 18-bit-wide to optimize the use of the target Field Programmable Gate Array (FPGA) high speed multipliers.

Using feedback control alone, it will not be possible to reach the required field amplitude and phase stability due to beam transient effects. Therefore, beam loading compensation is planned using timing-based feedforward control. To realize this, the timing system needs to reliably distribute the planned beam pattern at a rate of 250 Hz to the controller. Additionally, Beam Position Monitor (BPM) electronics can provide real-time information to the LLRF system to compensate the field for variations in phase and amplitude of the beam [7]. Adaptive feedforward is foreseen to compensate residual uncertainties in the RF chain [8, 9].

Bandwidth and Detuning Estimation For superconducting cavities, a real-time estimation of detuning and stored energy is required to implement a feedback controller for the piezoelectric tuners. Furthermore, the estimated cavity bandwidth can be used to implement a threshold-based quench detector. To perform these tasks, a model-based estimator is being adopted [10]. Since this kind of algorithm has been shown to be sensitive to transmission-line directional coupler finite directivity, a digital signal decoupler is planned to correct the recorded forward and reflected RF signals [11, 12]. The directivity of the directional coupler is going to be equal to or better than 35 dB.

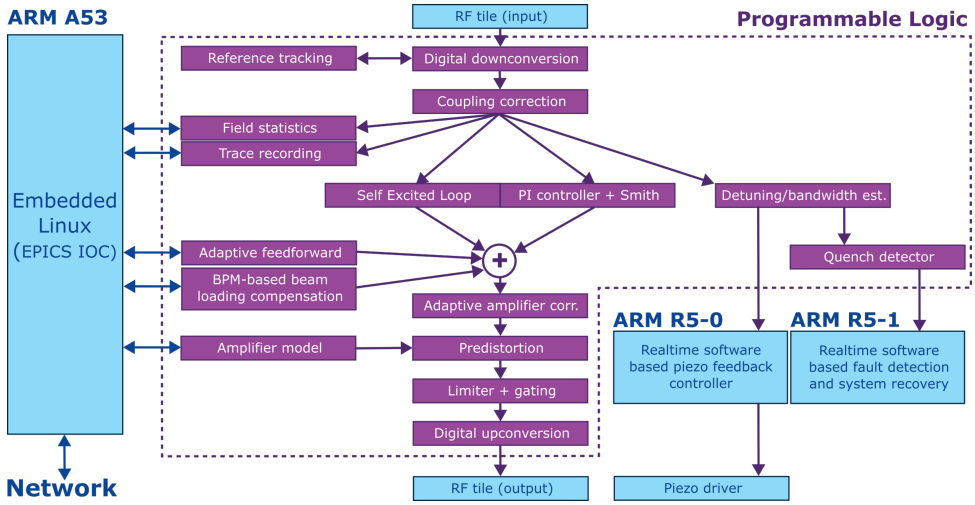

Figure 2: Block scheme of the LLRF system.

Detuning Control The resonance frequency of superconducting RF cavities is intended to be stabilized using control algorithms running on an ARM R5 real-time core.

An integral controller compensates slow detuning effects caused by cryogenic pressure drifts. The control bandwidth is limited to avoid exciting mechanical resonances of the cavity structure.

Periodic microphonics disturbances are intended to be suppressed using a Narrowband Active Noise Control (NANC) algorithm. The algorithm adapts the amplitude, phase and frequency of a numerically controlled oscillator to cancel sinusoidal detuning noise sources in the 0-200 Hz range [13].

Amplifier Linearization and Drift Compensation To validate the industrial use of ADSs, the machine must operate at maximum efficiency. Therefore, the drain voltage of each Solid State Amplifier (SSA) amplifier must be optimized to match the required power to drive a certain cavity be operated in nonlinear regime. This results in several degrees of phase shift due to amplitude-to-phase modulation that can degrade the regulation performance of the RF controller. A lookup table-based predistortion module is planned to compensate static nonlinearity [14]. Since the amplifier characteristics can drift due to environmental conditions, the LLRF architecture also includes an Output Vector Correction (OVC) unit to adaptively compensate residual plant mismatches [15].

Data Acquisition The decimated RF signals are intended to be continuously stored using a double-buffering scheme directly in the A53 processor memory. A dedicated FPGA module is being developed to compute statistical metrics such as mean, variance and power levels for selected RF signals. This allows real-time monitoring while reducing CPU processing load and data movement.

Upon an interlock event, high-resolution signal data surrounding the fault is intended to be stored in a circular buffer located in the FPGA DDR. This data enables detailed offline analysis of system failures.

Fault Recovery and Monitoring Upon a fault of an accelerating station, part of the machine is intended to be automatically re-configured to be able to generate the beam within 3 s. The affected cavities need to ramp down to allow the re-adjustment of the SSA drain voltage and then be switched back on with the new gradient. To achieve determinism in the reconfiguration procedure, one Cortex-R5 core of the RFSoC is intended to be used to automate setup tasks. Besides configuration tasks, this core is intended to actively monitor the status of the RF hardware and detect potential faults in the station.

CONCLUSION

Currently, the LLRF system for MYRRHA Phase 1 is in the implementation and early integration phase. Since the DAMC-DS5014DR board for the final accelerator installation is still in development at the moment of writing, the prototype board RFSoC4x2 from RealDigital [16] is being used for the initial development of the cavity controller. This board uses the same SoC family as the DAMC-DS5014DR and is supported by the DESY firmware framework, thus facilitating porting the code between the two. At the present stage, the main control and signal-processing functions are being developed and validated independently, while system-level integration on the prototype platform remains ongoing. The first validation tests will focus on RF feedback only and will be carried out on normal-conducting cavities. To validate the chosen solutions, it is planned to use a simulator-in-the-loop strategy. Furthermore, the normal-conducting (ATHENA) and superconducting (FREIA) test facilities will also support the R&D efforts of the MYRRHA LLRF control system with its first deployment by the end of 2026.

ACKNOWLEDGEMENTS

We express our gratitude to H. Schlarb, J. Branlard, M. Fenner, B. Boghrati, C. Guemues, P. Huesmann and P. Nonn of DESY for their invaluable feedback.

REFERENCES

[1] U. Dorda and A. Fabich, "Implementation status of MYRRHA phase 1 (MINERVA)", *J. Phys.: Conf. Ser.*, vol. 2687, no. 5, p. 052007, 2024. doi:10.1088/1742-6596/2687/5/052007

[2] S. Jablonski *et al.*, "High-speed ADC and DAC MicroTCA.4 AMC-RTM pair for diagnostics and feedback implementations", pp. 402–405, 2024. doi:10.18429/JACoW-IBIC2024-WEP55

[3] J. Georg *et al.*, "Board bring-up with FPGA framework and ChimeraTK on Yocto", pp. 557–560, 2023. doi:10.18429/JACoW-ICALEPCS2023-MO4AO03

[4] L. Butkowski, A. Bellandi, B. Dursun, C. Gümüş, and K. Schulz, "The DESY open-source FPGA framework", pp. 222–227, 2023. doi:10.18429/JACoW-ICALEPCS2023-MO4AO03

[5] D. Schulze, "Ponderomotorische stabilität von hochfrequenzresonatoren und resonatorregelungssystemen", Ph.D. thesis, Gesellschaft für Kernforschung mbH, Karlsruhe, Germany, 1971.

[6] N. Gandolfo *et al.*, "Development and performance of spoke cavity tuner for the MYRRHA linac project", pp. 667–670, 2019. doi:10.18429/JACoW-SRF2019-TUP087

[7] L. Butkowski *et al.*, "Implementation of the beam loading compensation algorithm in the LLRF system of the European XFEL", in *Proc. LINAC'18*, pp. 594–597, 2018. doi:10.18429/JACoW-LINAC2018-TUPO132

[8] C. Schmidt, "RF system modeling and controller design for the European XFEL", Ph.D. thesis, DESY, Hamburg, Germany, 2011. doi:10.3204/PHPPUBDB-17934

[9] S. Pfeiffer, "Symmetric grey-box identification and distributed beam-based controller design for free-electron lasers", Ph.D. thesis, Hamburg University of Technology, Hamburg, Germany, 2014.

[10] B. Richter *et al.*, "Estimation of superconducting cavity bandwidth and detuning using a Luenberger observer", *arXiv*, 2025. doi:10.48550/arXiv.2506.21207

[11] F. Qiu *et al.*, "Approach to calibrate actual cavity forward and reflected signals for continuous wave-operated cavities", *Nucl. Instrum. Methods Phys. Res. A*, vol. 1034, p. 166769, 2022. doi:10.1016/j.nima.2022.166769

[12] A. Bellandi, J. Branlard, M. Diomede, M. Herrmann, S. Pfeiffer, and C. Schmidt, "Calibration of superconducting radio-frequency cavity forward and reflected channels based on stored energy dynamics", *Nucl. Instrum. Methods Phys. Res. A*, vol. 1069, p. 169825, 2024. doi:10.1016/j.nima.2024.169825

[13] A. Bellandi *et al.*, "Narrow bandwidth active noise control for microphonics rejection in superconducting cavities at LCLS-II", *arXiv*, 2022. doi:10.48550/arXiv.2209.13896

[14] A. Bellandi *et al.*, "Results on FPGA-based high-power tube amplifier linearization at DESY", *IEEE Trans. Nucl. Sci.*, vol. 67, no. 5, pp. 762–767, 2020. doi:10.1109/tns.2020.2980929

[15] M. Omet *et al.*, "LLRF operation and performance at the european XFEL", pp. 1934–1936, 2018. doi:10.18429/JACoW-IPAC2018-WEPAF051

[16] *RFSoC 4x2 development board*, Real Digital, 2024. https://www.realdigital.org/hardware/rfsoc-4x2