UPGRADE OF THE BEAM LOSS MONITORING SYSTEM FOR THE UNILAC HEAVY ION LINEAR ACCELERATOR AT GSI

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Abstract

The beam-loss monitoring system of the UNILAC heavy-ion linear accelerator is based on measuring the beam current at multiple locations along the beamline. Signals from beam–current transformers are amplified, converted into pulse trains and counted within a defined time window. The system has proven to be robust and operationally safe.

The ongoing upgrade aims to replace the current-to-frequency converters and the entire digital subsystem while preserving the established operational principle and the analog front-end. Most important reasons are aging of the electronics, the need for improved scalability, flexibility and safety, and last but not least, alignment with the new GSI/FAIR controls architecture.

The new system operates under the supervision of a System Control Unit (SCU), the standard front-end platform of the GSI/FAIR control system. It is controlled by the Front-End Software Architecture (FESA) and White Rabbit. Once configured, the FPGA-based hardware operates autonomously to ensure high reliability and fail-safe behaviour.

Here we describe the system architecture, its modular hardware, firmware architecture and the software interface.

INTRODUCTION

The beam loss monitoring (BLM) system was introduced to the UNILAC accelerator as part of the upgrade programme for high-current operation of the accelerator by late 1990s [1]. The system uses multiple beam-current transformers [2] at various locations along the accelerator [3]. Transformer signals are amplified by calibrated front-end amplifiers, and the resulting voltages are converted to pulse trains using voltage-to-frequency (V→f) converters. These signals are fed to differential integrators based on digital up/down counters as shown in Fig. 1. If the resulting count within a single beam pulse exceeds a prescribed threshold, the BLM triggers the chopper control circuitry to truncate the beam pulse.

The operation of amplifiers and counters is subject to gate signals to eliminate interferences outside the beam pulse window. A special version of the integrator with only a single, up-counting input is used to control overall beam charge for profile harp protection.

With the concept of *virtual accelerators* at UNILAC [4], various species can be accelerated in adjacent 20 ms-long cycles. To accommodate the required threshold changes, the threshold registers are reloaded at the beginning of each cycle.

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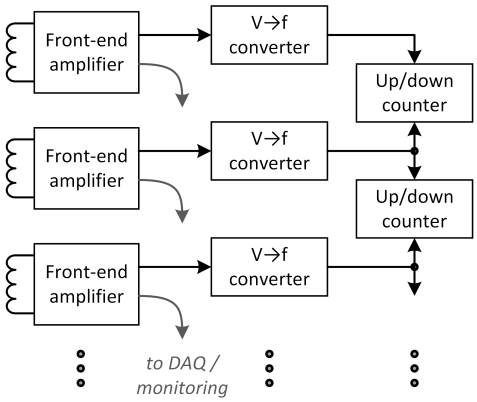

Figure 1: Simplified signal processing flow.

The original BLM system demonstrated robust operation for over 25 years. However, further maintenance and system extensions became impossible due to its ageing design and the lack of legacy electronic components. This factor, coupled with a growing need for a direct, modern interface to the new control system, necessitated a major upgrade.

SCOPE OF THE UPGRADE

The upgrade includes the replacement of the V→f converter electronics, the entire digital section and the control software. The overall principle of operation, the beam transformers and the proven front-end amplifiers remain unchanged.

The hardware changes affect the resolution and range of the system as shown in Table 1.

Table 1: BLM Parameters Before and After Upgrade

Parameter	Original	Upgraded
Resolution	2.2 nC	0.7 nC
Max. pulse frequency	8 MHz	24 MHz
Counter depth [bits]	13 + sign	31 + sign
Counting range	±18.022 µC	±1.5 C [1]

The functions of the V→f converter and the counter, originally implemented in a single device, have been split into separate hardware crates.

The *V→f converter crates* contain custom modules designed specifically for the BLM. The *counter crates* are built from standard hardware components used at the GSI control system, avoiding dedicated hardware development.

The upgraded system is largely scalable and imposes no inherent limits on the number of input signals.

[1] Practical range is limited to <100 µC by max. pulse frequency and beam pulse duration.

V→F CONVERTERS

The operation principle of the V→f converter is illustrated in Fig. 2: it is a synchronous, first-order, one-bit ΔΣ modulator. The output (and feedback) is gated with the clock signal to get discrete pulses rather than a continuous binary waveform.[2]

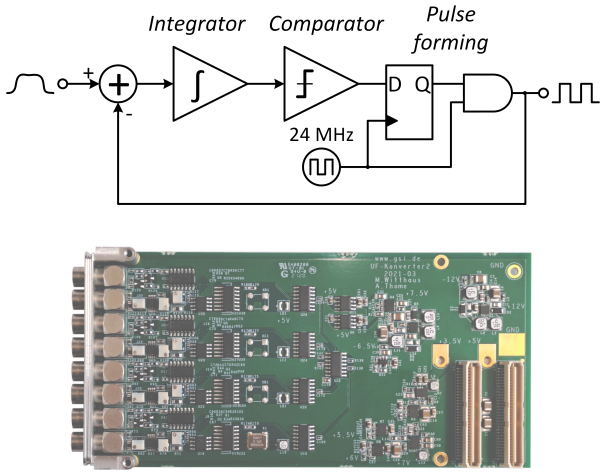

Figure 2: Operation principle (top) and the PCB view (bottom) of the V→f converter.

The circuit uses discrete components as no single-chip solutions with comparable performance have been found on the market. Four channels are implemented on a PMC-format board and are designed for installation in a μTCA crate. A single crate contains up to 8 modules, giving a total of 32 channels.

COUNTER CRATE

The two main components of the counter crate are the System Control Unit (SCU) and the Digital I/O Board (DIOB) as shown in Fig. 3.

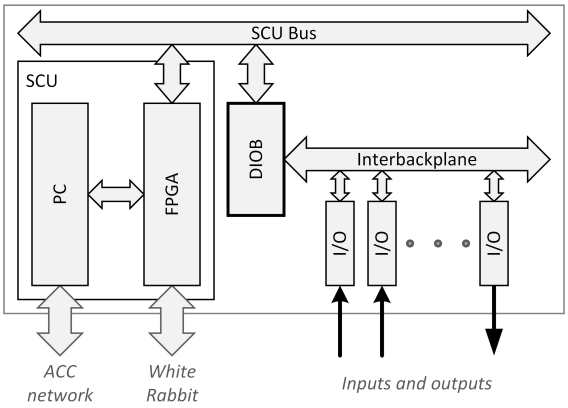

Figure 3: The counter crate including an SCU, DIOB and I/O modules.

The SCU [5, 6] is a common frontend controller at GSI. It contains an embedded PC running the control software and an FPGA-based circuitry which acts as a timing receiver and local bus interface.

The DIOB is a universal, FPGA-based module for implementing use-case-specific, real-time functionality. It communicates with up to 12 I/O modules with 6 inputs or outputs each. The counter crate is equipped with 8 fast input modules for V→f pulses, 2 isolated input modules for gates and 2 output modules to trigger the chopper control.

The structure of the DIOB gateware is shown in Fig. 4. The key idea is to use a flexible *counter pool* containing multiple, identical up/down counter units. Inputs of the counters can be freely connected to signal inputs via a configurable *input patch matrix*. The same philosophy is used for gate inputs (not shown in the figure) and outputs to the chopper control. Such an architecture allows on-the-fly reconfiguration — which was not possible with the original system.

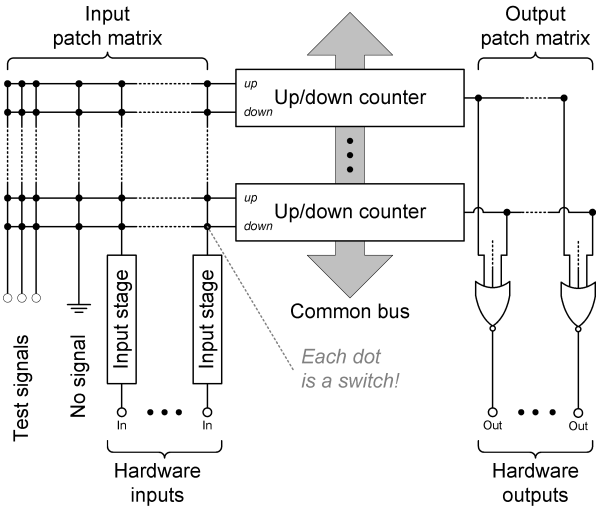

Figure 4: The counter pool with patch matrices - a simplified block diagram.

A single up/down counter unit contains the counter, two threshold registers and two comparators: for the positive and the negative threshold.

To support Unilac's architecture containing multiple, partly independent sections, each counter can be assigned to one of 16 *groups*. Further, up to 64 full sets of threshold data (*datasets*) can be stored in a local memory to facilitate fast switching according to the virtual accelerator philosophy. The datasets can be switched per-group directly by the SCU's timing receiver, without the interaction with software, which guarantees robustness and deterministic response time.

The signal input stages shown in Fig. 4 provide signal debouncing (which limits the input frequency to 31.25 MHz) and a watchdog: the V→f converters generate certain idle frequency even with zero input. Lack of this signal is used to detect connection loss.

Gate signals are supplied by hardware, isolated TTL inputs. A safety mechanism triggers if an expected gate pulse is missing or a pulse arrives unexpectedly.

A single counter crate supports up to 48 input signals, 12 gate inputs and 12 outputs to the chopper control.

[2] Note that gating the feedback signal does not change the operation principle of the modulator.

SOFTWARE AND INTEGRATION

The control software is based on the Front-End Software Architecture [7, 8] (FESA) and runs under control of an embedded Linux system [9] within the SCU.

The control system architecture assumes that every counter is a separate device (which was the case of the original BLM) while the hardware integrates multiple counters into one entity. This discrepancy has been addressed by introducing *virtual devices* and dividing the software into two layers:

- The *interface layer* provides one instance per virtual device and covers FESA communications, data conversion and provides a device model for the control system.
- The *frontend layer* is responsible for configuring the counter pool by assigning inputs, outputs and threshold values, and configuring timing events for beam-synchronous operation. It governs communication with the hardware in order to allow safe, atomic access and undisturbed handling of the timing events. Further, it performs continuous data acquisition and buffering. The frontend layer hides most of the low-level complexity, providing only the necessary interface.

COMMISSIONING

Due to its relevancy to machine safety, the BLM system has been tested on various stages of development. This included:

- Tests of the counter crate with artificial signal patterns;
- Tests of the counter crate along with V→f converters using artificially generated analogue signals — see Fig. 5;

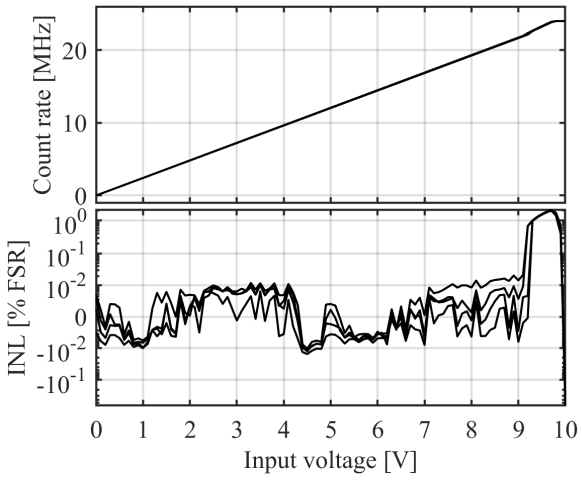

Figure 5: Static characteristics (top) and integral nonlinearity (shown in quasi-logarithmic scale [10], bottom) of the V→f converters, measured for 4 channels.

- Beam tests to assure proper real-time operation, check the data acquisition and collect data for further evaluation.

The next planned step shall be parallel operation of the new system along with the original one to compare them directly during the beam time. However, probable irreversible damage to the original system due to the fire incident at GSI in February 2026 will force these plans to be revised.

CONCLUSION

While the new BLM system for Unilac is not revolutionary compared to the original solution, it represents an advance in terms of applied technology, software interface and working parameters. Its flexibility will allow easier adjustments and future expansion. Use of modern hardware solutions shall guarantee its maintainability over the next two decades.

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