# HIGH-PRECISION CURRENT FEEDBACK CONTROL OF A MHz KICKER MAGNET SYSTEM FOR THE SHINE

S. Li[1], Y. Liu[1], Y. Jiang[1], R. Wang[1], W. Zhang[1], H. Deng[1], Q. Yuan[1†]
[1]Shanghai Advanced Research Institute, Chinese Academy of Sciences, Shanghai, China;

*Abstract*

A kicker magnet system is under development for the Shanghai High Repetition Rate X-ray Free~~-~~-Electron Laser and Extreme Light Facility (SHINE) at the Shanghai Advanced Research Institute, Chinese Academy of Sciences (SARI, CAS). Mitigating thermal drift during extended operation is essential ~~to~~ for maintaining the beam distribution stability. A high-precision current-feedback control system has been designed to regulate the kicker power supply at 1 MHz with an amplitude stability below 100 ppm. The system integrates a differential amplification circuit using a low-thermal-coefficient resistor network for real-time drift compensation, together with a proportional–integral–derivative (PID) controller operating at a response time of ~100 ms to stabilize the output current. This approach provides a voltage measurement resolution on the order of 0.1 mV. Under 1 MHz pulsed operation, the experimental results achieve a pulse-to-pulse amplitude stability of 85 ppm over 30 minutes with closed-loop feedback, and maintain stability around 111 ppm after 8 hours of continuous running. The design, implementation, and tested performance of the system are reported and discussed.

## INTRODUCTION

The Shanghai High Repetition Rate X-ray Free-Electron Laser and Extreme Light (SHINE) facility is under construction based on the superconducting linear electron accelerator ~~facility~~ at the Shanghai Advanced Research Institute (SARI), Chinese Academy of Sciences (CAS). It generates a maximum energy of ~~up to~~ 8 GeV at a high repetition rate of 1 MHz. A pulsed power system provides the required pulsed excitation current for the kicker magnet (a dummy load in this case) to ~~maintain~~ control the electron-beam trajectory variation~~s of the electron beam~~. The inductively loaded kicker system consists of a charging current power supply (CCPS), an energy storage ~~unit~~, a pulser ~~unit~~, a programmable logic controller (PLC) ~~unit~~, and an inductive magnet.

The kicker system outputs consecutive quasi-half-sinusoidal ~~half quasi-sinuous~~ waveforms – with a peak current up to 54 A (~~A~~ corresponding to a 2.7 V output amplitude into 50 Ω ~~is obtained~~ with a current transducer of 0.05 V/A sensitivity), a pulse width of approximately~~around~~ 450 ns, and a flat-top width of 10 ns – at a ~~maximum~~ repetition rate up to 1 MHz with a desired stability of less than 100 ppm when driving ~~loaded with the~~a magnet load of ~~at an inductance of~~ 1.6 μH [1]. The above requirements ~~have~~ pose~~d a~~ significant challenges ~~to controlling~~for the control of the kicker system ~~in order~~ to fulfil~~l~~ the design criteria of the SHINE facility. In particular, the amplitude stability of the kicker is fundamental for precise beam switching and transport, as thermal drift is expected ~~to occur~~ over extended operation.

Several studies have been carried out to investigate the feasibility of improving the stability of pulsed power supplies [2-7]. At PSI, a balanced measurement scheme comprising balancing, limiter, and amplifier circuits was designed. Digital peak detection was implemented in a field-programmable gate array (FPGA), and the maximum pulse value was sent to a microcontroller system [2]. The peak-to-peak stability was ±~~-~~11 ppm with active feedback control. At SACLA, a feedback control system consisting of a current transducer, an error amplifier, and a proportional-integral-derivative (PID) control circuit was designed to stabilize the output current within 5 mA, and a pulse-width modulation (PWM) module was employed for gate control of the fast switching [3,4]. In reference [5], the measured current was regulated using a reference signal tracking (RST) tri-polynomial form and processed in a digital signal processing controller. A ~~similar~~ control ~~method~~approach similar to that in [2] was applied for the digital control electronics at SOLEIL and HEPS, with closed-loop regulation implemented in an FPGA [6, 7]. The control methods mentioned above primarily rely on closed-loop PID control implemented in an FPGA, RST digital control, or a combination thereof. ~~Other m~~ More complex control methods, such as model predictive control [8, 9], adaptive control [10, 11], and analytical model-based optimal control [12], have also been reported.

The primary technical challenge is the sub-microsecond latency constraint at 1 MHz: a 450-ns pulse width leaves a net interval of ~550 ns, of which only 300–400 ns is available for closed-loop correction after accounting for analog-to-digital conversion (ADC) and processing delays – precluding conventional data acquisitions [2, 5]. Addressing this requires a tightly synchronized FPGA architecture with high-bandwidth analog conditioning. In this work, a novel continuous chopping amplifier ~~circuit design~~ is proposed to enable high-precision measurement of the kicker's voltage amplitude, thereby providing an accurate voltage reference at each iteration. While closed-loop control enables consistent pulse-to-pulse correction, minor voltage or current variations in the kicker output can~~not~~ be discriminated~~distinguished~~ from the amplifier's inherent zero-drift ~~of the amplifier~~, ~~and~~ moreover, flicker noise is also mitigated. ~~Controlling~~ Regulating the charging voltage of the CCPS – which is proportional to the excitation pulse current – through a high-speed closed-loop helps reduce thermal drift of the overall system during extended operation.

†yuanqb@sari.ac.cn

## MATERIALS AND METHODS

### *Current feedback control overview*

The current feedback control system consists of a pulse detection circuit, a dual-channel 16-bit ADC board, an FPGA core board, and a digital-to-analog converter (DAC) board. The two ADC modules are connected to the FPGA core board, which provides the necessary resources and interfaces for data acquisition, processing, and monitoring. The DAC board supplies analog output channels to close the overall ~~system's~~ control loop. The 1 MHz quasi-half-sinusoidal waveform~~quasi-half-sine wave~~ is resistively balanced against a high-stability DC reference to generate a differential signal for further amplification.

Data from 50 consecutive 450-ns kicker cycles (160 points each) ~~formed~~ were organized into a 50×160 array. Three peak values per cycle were extracted, sorted, and trimmed to the central 20 by discarding the outermost 130 values. Stability was evaluated as the ratio of the standard deviation-to-mean ~~ratio~~ of these refined points. A LabVIEW interface (National Instruments, U.S.A.) was developed for data monitoring and transfer. The PID control is implemented by configuring several key parameters, as illustrated in Fig. 1.

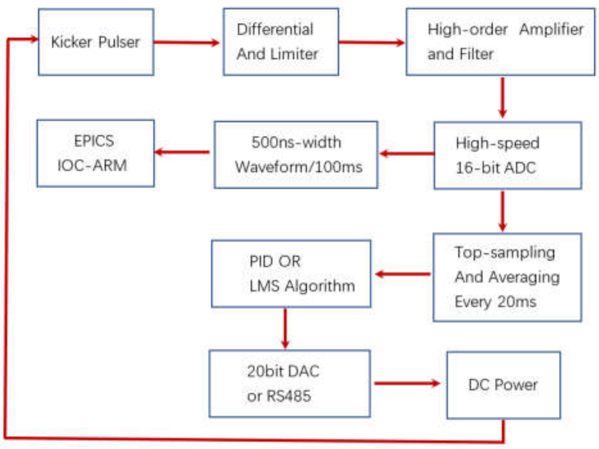


Figure 1: A diagram of the current feedback control for the kicker at SHINE.

### *Mechanical design*

The current feedback control system is designed as a standard 1U ~~rack~~ chassis (dimensions: 482.6 mm~~ width~~ × 400 mm~~ depth~~ × 44 ~~mm~~ mm, W×D×H~~height~~) for ease of maintenance. It is installed in a standard 19-inch cabinet together with a PLC controller to ~~avoid~~ minimize radiation damage. Each board is ~~independently~~ implemented as a standalone module~~designed~~ to facilitate easy debugging and replacement. ~~An~~ The internal layout is shown in Fig. 2 for further clarity.

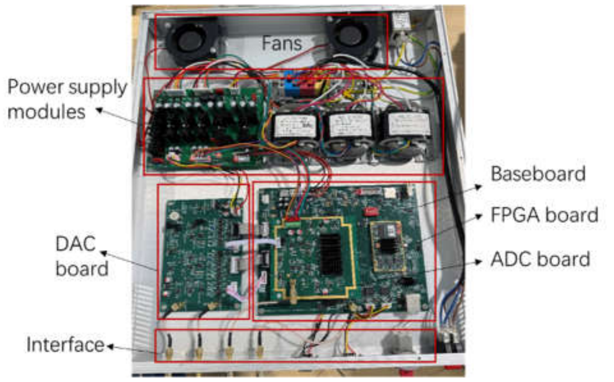


Figure 2: Internal layout of the feedback controller for the kicker.

### *Experimental measurements*

Measurements were performed to characterize the full and amplified waveforms ~~across~~ over a frequency range of 1 Hz ~~to~~ – 1 MHz, as well as to evaluate system resolution and pulse-to-pulse stability. Generally, a signal generator (Agilent 33500B Series, 16-bit) was used to directly provide a DC signal to verify~~, enabling verification of~~ the ~~feedback~~ controller's ~~capability~~ ability to detect the minimum resolvable voltage step~~ change~~. Pulsed current measurements were carried out using an internal wide-band current transducer (Pearson model 6600, U.S.A.) with a sensitivity of 0.1 V/A, a maximum RMS current rating ~~up to~~ of 40 A, and a bandwidth of up to 120 MHz.

## RESULTS AND DISCUSSIONS

### *Resolution measurement*

To distinguish the smallest voltage change, a resolution measurement was carried out using the method described in Section Experimental measurements. A DC voltage ranging from 2.376 V to 2.381 V was fed into the feedback controller with steps varying from ~~adjustments of~~ 1 mV down to 0.1 mV, and the ~~resulting~~ corresponding responses ~~curves~~ are shown in Fig. 3. As indicated in the ~~embedded~~ inset ~~plot~~ of Fig. 3, the 0.1 mV steps are clearly visible during the interval from 800 s to 900 s. In particular, the voltage peak at 2.3798 V confirms that the minimum resolvable voltage increment on the system readout is 0.1 mV.

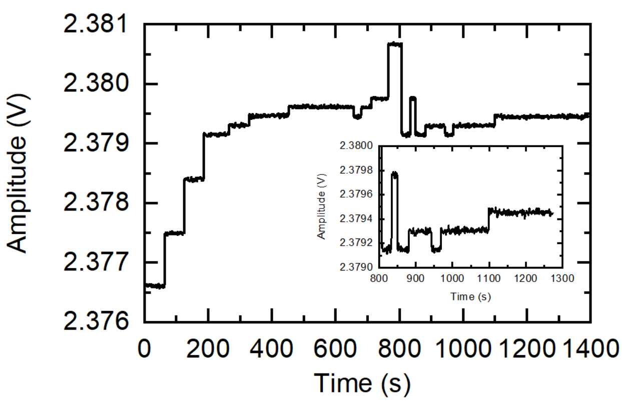

Figure 3: Resolution measurements at a voltage step of 1 mV – 0.1 mV.

### *Short-term stability measurement*

Fig.~~ure~~ 4 provides the overall measurement results – including waveform acquisition, PID configuration, and key parameters – obtained at a charging voltage of 800 $V_{DC}$ and a repetition rate of 1 MHz with feedback control enabled. Data were recorded every 50 ms for subsequent comparison. Here, the 'full-voltage' is the amplitude of the entire waveform, while the 'cut-voltage' corresponds to the amplitude of the locally amplified segment. The full waveform ~~shows~~ exhibits a width of 452 ns and a voltage amplitude of 1.32 V. A 0.15 V signal is amplified with a gain of 12. The measured stability is 85 ppm (RMS) with the designed feedback control based on the amplified-voltage method, representing a significant improvement compared to the open-loop operation [1].

The dynamic process of stability improvement is illustrated as follows: (i) the PID control rapidly suppresses voltage fluctuations during the pulse flat-top, with the waveforms settling to the target value within approximately 100 ms; and (ii) the integral (I) term compensates for baseline drift caused by slow variations such as temperature changes and component-parameter shifts from pulse-to-pulse, thereby ensuring consistent energy per pulse. These results indicate that the kicker system, under closed-loop control, exhibits a sufficiently fast response time ~~sufficiently fast~~ to maintain the target value.

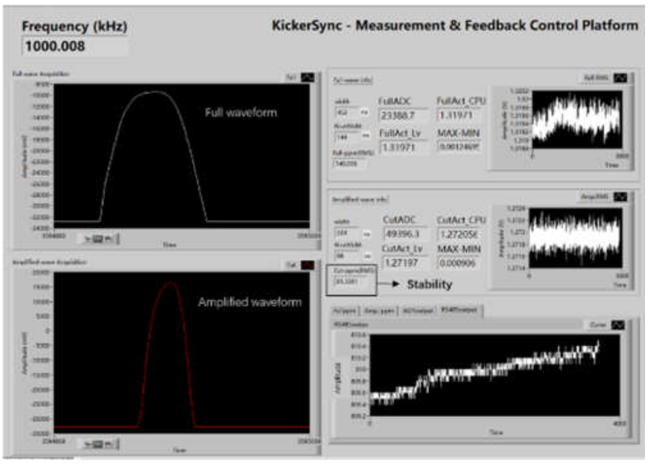


Figure 4: Short-term stability measurement over 30 min with feedback control.

### *Long-term stability measurement with feedback*

To ensure safe commissioning, the PID output voltage was constrained to the range of 750 V to 850 V. The PID ~~coefficients~~ gains were set to P = 0.8 and I = 2 for evaluating the closed-loop performance. The closed-loop feedback control is employed to correct amplitude drift and reduce temperature-induced drift ~~through~~ by continuously compensating based on the ~~compensation of~~ voltage measurement~~s~~. The results are plotted in Fig. 5, showing the variation of the DC power-supply output voltage, kicker pulse amplitude, and the resulting stability over an 8-hour period ~~hours~~.

As shown in Fig. 5, the stability ~~trend~~ shows a gradual, monotonic drift toward a new equilibrium over the subsequent hours. After 8 hours of continuous operation, the system achieved a stability of approximately 111 ppm RMS, meeting the design requirements outlined in prior work [1].

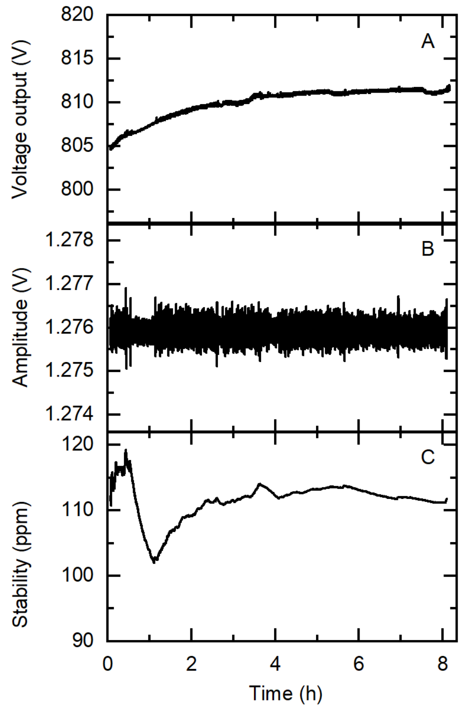


Figure 5: Long-term stability measurements of closed-loop, including voltage output (A), amplitude (B), and stability (C).

## CONCLUSIONS

In this work, a prototype ~~of a~~ high-precision current feedback controller for a kicker power supply operating at a repetition rate of 1 MHz was designed. Preliminary results demonstrated a voltage measurement resolution ~~in~~ at the sub-ppm level for a 0.1 mV step. Under closed-loop ~~feedback~~ control at 1 MHz ~~repetition rate~~, pulse-to-pulse amplitude stabilities of 85 ppm (over 30 minutes) and 111 ppm (after 8 hours) of continuous operation were achieved. The development of the current feedback controller ~~confirms that the performance~~ meets the design targets and demonstrates the ability to ~~mitigate~~ suppress thermal drift during long-term operation.

Further measures are being implemented to enhance performance, including: (i) adopting a master timing reference for synchronization in subsequent processing algorithms – ~~—~~once synchronized, a fixed sampling point can serve as a reference, eliminating the need for multi-~~data~~ sample averaging in the current calculation~~s~~; and (ii) incorporating fault-diagnosis information such as waveform distortion, timing jitter, and vibration.

## REFERENCES


[1] Y.-F. Liu, M. Gu, Q.-B. Yuan, R. Wang, J. Tong, and S. Li, "Development of a MHz Pulsed Power Supply for Kicker Magnet in SHINE," IEEE Trans. Power Electron., vol. 39, no. 4, pp. 4291–4300, Apr. 2024. doi:10.1109/tpel.2023.3347748

[2] M. Paraliev and C. H. Gough, "Resonant Kicker System with Sub-part-per-million Amplitude Stability", in Proc. IPAC'17, Copenhagen, Denmark, May 2017, pp. 3174-3177. doi:10.18429/JACoW-IPAC2017-WEPIK098

[3] C. Kondo et al., "High-Precision Pattern Power Supply of Kicker Magnet for Multi-Beamline Operation at SACLA", in Proc. IPAC'17, Copenhagen, Denmark, May 2017, pp. 3404-3407.doi:10.18429/JACoW-IPAC2017-WEPVA061

[4] K. Tono, T. Hara, M. Yabashi, and H. Tanaka, "Multiple-beamline operation of SACLA," J Synchrotron Rad, vol. 26, no. 2, pp. 595–602, Feb. 2019. doi:10.1107/s1600577519001607

[5] S. Yammine and H. Thiesen, "HL-LHC Inner Triplet Powering and Control Strategy", in Proc. IPAC'17, Copenhagen, Denmark, May 2017, pp. 3544-3546. doi:10.18429/JACoW-IPAC2017-WEPVA116

[6] F. Bouvet et al., "Innovative Design of the Fast Switching Power Supplies for the SOLEIL EMPHU Insertion and its Fast Correctors", in Proc. IPAC'11, San Sebastian, Spain, Sep. 2011, paper TUODB03, pp. 982-984.

[7] F. Long, Y. P. Liu, X. Qi, and Z. H. ZhenHua, "Conceptual Design for the HEPS Power Supply System", in Proc. IPAC'16, Busan, Korea, May 2016, pp. 3540-3542. doi:10.18429/JACoW-IPAC2016-THPMW004

[8] C. Xu et al., "Efficient data-driven model predictive control for online accelerator tuning", in Proc. IPAC'25, Taipei, Taiwan, Jun. 2025, pp. 2931-2934. doi:10.18429/JACoW-IPAC2025-THPM116

[9] S. Appel, S. Hirlaender, and N. Madysa, "Data-driven model predictive control for automated optimization of injection into the SIS18 synchrotron", in Proc. IPAC'24, Nashville, TN, USA, May 2024, pp. 1800-1803. doi:10.18429/JACoW-IPAC2024-TUPS59

[10] A. Scheinker, "Adaptive Control and Machine Learning for Particle Accelerator Beam Control and Diagnostics", in *Proc. IBIC'21*, Pohang, Korea, Sep. 2021, pp. 466-472. doi:10.18429/JACoW-IBIC2021-THOB03

[11] C. Emma, A. Edelen, M. J. Hogan, B. O'Shea, G. White, and V. Yakimenko, "Machine learning-based longitudinal phase space prediction of particle accelerators," *Phys. Rev. Accel. Beams*, vol. 21, no. 11, Nov. 2018. doi:10.1103/physrevaccelbeams.21.112802

[12] X. Wang, Y. Huang, W. Shen, F. Wu, and D. Gao, "Analytic Modeling Optimal Control of Pulsed Power Supply for Accelerator Magnet," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5657–5665, Jul. 2020. doi:10.1109/tie.2019.2934025