

ANALOG DOWN-CONVERSION AND DIGITAL READOUT SYSTEM FOR A CAVITY BPM BEAM TESTED AT ATF

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Abstract

A complete analog readout system designed to extract reference and position signals from a single cavity Beam Position Monitor (cBPM) has been developed for a prototype from CEA Saclay. The complete system underwent beam testing at the Accelerator Test Facility (ATF). The monitor operates with a dipole mode centered at 1.725 GHz, requiring translation to lower frequencies for digitization and subsequent signal processing via a digital-down-conversion (DDC) algorithm. Throughout beam campaigns in May, June, and December 2025, various synchronized local oscillator (LO) configurations and down-conversion architectures were evaluated.

The final optimized systems achieved intermediate frequencies (IF) of 417 MHz, 297 MHz, and 60 MHz. Through iterative enhancements in synchronization, filtering, and hardware integration, a peak vertical resolution of 2.81 μm was demonstrated.

INTRODUCTION

High-resolution Beam Position Monitors (BPMs) are essential diagnostics for contemporary and next-generation particle accelerators. In linear collider applications, the preservation of ultra-low emittance beams requires sub-micrometric transverse position measurements.

Cavity BPMs are well suited for this purpose because they exploit resonant electromagnetic modes excited by the beam. In this scenario, the monopole mode provides a charge normalization and phase reference, whereas the amplitude and phase of the dipole mode encode the beam's spatial displacement. Given that the resulting RF output typically resides in the GHz range, these signals cannot be directly processed by standard digitizers.

Therefore, analog down-conversion electronics are required to translate the cBPM signals to a lower intermediate frequency (IF), relaxing ADC sampling constraints while preserving the amplitude and phase information within the acquired waveforms. This work details the development and beam-based validation of a fully synchronized readout chain for a CEA Saclay re-entrant cBPM prototype [1] commissioned at ATF Linac.

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TESTED CBPM PROTOTYPE

The cBPM under evaluation is a re-entrant resonator with operating frequencies 1.250 GHz and 1.725 GHz for the monopole TM_{010} and dipole TM_{110} modes, respectively. The amplitude of the dipole signal is proportional to beam offset (δx) and bunch charge (q_{bunch}):

$$V_{\text{TM}110} \propto q_{\text{bunch}} \cdot x. \quad (1)$$

To achieve position independence from charge fluctuations, the monopole mode signal which scales solely with q_{bunch} is used for normalization. Additionally, the monopole mode also provides a phase reference which enables the detection of the sign of the beam displacement [2]. This resonant monitor exhibits relatively low loaded quality factors, measured via a Vector Network Analyzer (VNA) at $Q_L = 30.99$ for the monopole mode and $Q_L = 46.40$ for the dipole mode. A low quality factor implies broadband cBPM signals and a rapid decay time of approximately 30 ns to 40 ns (following analog processing).

The BPM prototype was installed at the end of the ATF linac at KEK for beam testing. The ATF facility provides an RF reference signal of 714 MHz, the fourth harmonic of the RF Main Linac frequency of 2856 MHz [3]. Precise synchronization of the local oscillator with this reference is imperative to maintain phase stability across successive bunch measurements. This synchronization is especially critical given the broadband nature of the resonances; the rapid decay of the cBPM waveforms renders the peak amplitude measurement highly sensitive to the IF phase.

ANALOG DOWN-CONVERSION SYSTEM

The readout system was designed to extract both position and reference information from a single cBPM. The broadband nature of the signals allow for the extraction of the monopole mode at the frequency of the dipole mode.

The four BPM outputs are combined using 180° hybrid couplers to generate horizontal and vertical position channels (derived from the Δ ports), and a reference channel (derived from the Σ port). Three identical processing chains are implemented to handle these signals. An initial band-pass filter (BPF) centered at the dipole mode frequency selects the signal of interest for the position channels (removing higher order modes). For the reference channel, this BPF isolates

the spectral tail of the monopole mode that overlaps with the dipole frequency. Additional RF stages, including attenuators, low-noise amplifiers, mixers, and IF conditioning filters, are employed to prepare the signal for digitization.

Several LO frequencies—and their corresponding IF were evaluated during beam operations to optimize spatial resolution. The components of the IF conditioning stage are selected according to the frequencies of the IF signal (Table 1).

Table 1: Parameters of the Evaluated Frequency Configurations

Setup	LO (GHz)	IF (MHz)
Initial setup	1.875	150
Optimized May setup	2.142	417
December setup A/B	1.428	297
December setup C	1.428 and 0.357	60

In the initial configuration, the LO was synthesized from the ATF 10 MHz master clock. However, with the LO operating at 1.875 GHz, the LO phase was found to be inconsistent at the arrival time of each bunch, leading to non-reproducible measurements. To resolve this, the reference input for the Phase-Locked Loop (PLL, LMX2592EVM) [4] was switched to the 714 MHz reference signal, which is an integer multiple of the 3.125 Hz bunch repetition frequency. This optimized setup ensures the LO is phase-locked to the ATF accelerator timing system.

The December configurations A, B, and C were re-designed by modifying the RF components and the hardware arrangement was enhanced to improve robustness (Fig. 1). For these configurations, the LO frequencies are precisely selected to ensure phase-locked synchronization with the beam arrival time at a repetition rate of 3.125 Hz. All experimental configurations corresponding to the month of December are presented in Fig. 1.

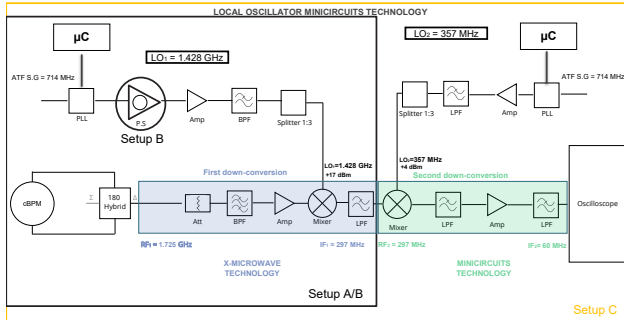


Figure 1: Schematic of the analog down-conversion chain and LO generation for setups A, B, and C.

While Setups A and B utilized identical frequency plans (1.428 GHz LO and 297 MHz IF), Setup B incorporated a manual phase shifter in the LO path. This allowed for fine phase tuning to maximize the IF signal amplitude during the window where the exponential envelope reaches its peak. Finally, Setup C introduced a dual-stage down-conversion;

the 297 MHz IF was mixed with a second local oscillator (LO2) at 357 MHz, resulting in a final IF of 60 MHz.

DIGITAL SIGNAL PROCESSING

For all configurations, the signals were digitized at a sampling rate of 2 GS/s using a RIGOL oscilloscope. A digital processing is implemented to extract amplitude and phase components, followed by normalization to isolate the position-dependent contribution. The phase difference between the dipole and monopole modes determines the direction of the beam offset relative to the electrical center of the cavity

To retrieve amplitude and phase from the digitized waveforms, a digital down-conversion (DDC) algorithm [5] is implemented to the IF signals. The waveforms are mixed down base-band using a numerical oscillation frequency ω_{DDC} and processed through a Gaussian filter g , leading to the complex DDC signal y_{DDC} . For digitized signal y with N samples, at sampling time t_j :

$$y_{DDC}(t_i) = \sum_{j=0}^{N-1} y(t_j) \cdot e^{-i\omega_{DDC}t_j} \cdot g(t_i - t_j). \quad (2)$$

From y_{DDC} one can obtain the amplitude A and phase ϕ information from position and reference signals:

$$A(t_i) = \sqrt{y_{DDC}(t_i) \cdot y_{DDC}^*(t_i)} \quad (3)$$

$$\phi(t_i) = \arctan \frac{\text{Im}(y_{DDC}(t_i))}{\text{Re}(y_{DDC}(t_i))}. \quad (4)$$

After normalization, one can obtain in phase I and in quadrature Q components at sampling point t_s :

$$I = \frac{A_p(t_s)}{A_r(t_s)} \cos(\phi_p(t_s) - \phi_r(t_s)) \quad (5)$$

$$Q = \frac{A_p(t_s)}{A_r(t_s)} \sin(\phi_p(t_s) - \phi_r(t_s)) \quad (6)$$

where the subscript p and r refer to the position and reference signals, respectively. In the IQ -plane, a concentrated cluster of points (as opposed to an elliptical distribution) serves as an indicator of system phase stability and measurement reproducibility (Fig. 2).

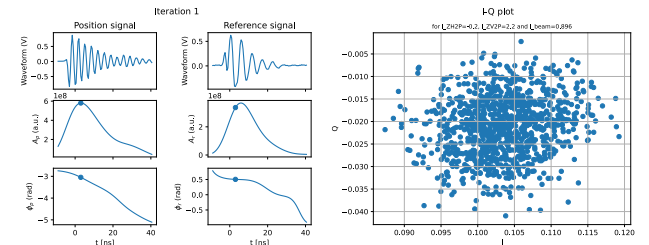


Figure 2: Implementation of the DDC algorithm for a single acquisition (left) and IQ -plot for a set of measurements (right).

A calibration procedure (Fig. 3) is applied to translate measures in terms of I and Q to beam position measurement.

By executing a sweep in estimated beam position (via upstream steering magnets), and a rotation in the IQ -plane, a measure P is obtained that depends exclusively on the beam offset in the targeted transverse plane. The linear regression between P and estimated beam position yields the calibration curve.

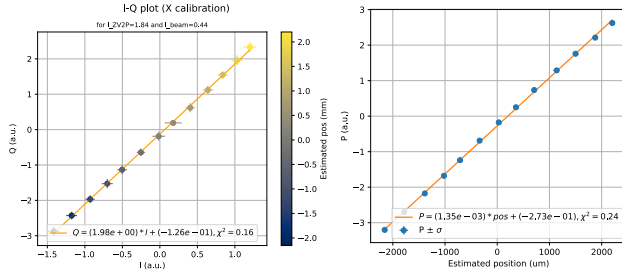


Figure 3: Calibration curves for the X-plane.

BEAM TEST RESULTS

To evaluate the system's performance, spatial resolution was determined using Model Independent Analysis (MIA) and Singular Value Decomposition (SVD) methods. The estimated beam position (reconstructed via the measurements of 10 stripline BPMs) is compared against the cBPM measured beam position. The root mean square (RMS) of the residuals serves as measurement of the spatial resolution [5]. Additionally, the calibration procedure provides information regarding the linearity and the dynamic range of the system.

Six experimental shifts were conducted during May and June 2025. Initial tests were primarily dedicated to troubleshooting LO synchronization and validating the digital signal processing software. After establishing stable LO phase-locking with the bunch arrival time, the peak resolutions recorded during the May/June period were $37.9 \mu\text{m}$ in the horizontal plane and $13.4 \mu\text{m}$ in the vertical plane.

Three additional shifts in were performed in December 2025 where, after reducing the IF frequencies and refining filtering stages, the horizontal measured resolution improved to $9.36 \mu\text{m}$. The vertical plane exhibited greater stability in beam jitter, therefore different configurations (setups A, B and C) were evaluated in this plane, leading to the resolutions summarized in Table 2.

Table 2: Measured vertical plane resolutions for the December 2025 configurations

Setup	Calibration fit		Resolution measurements		
	Dynamic range	χ^2	Bunch charge	Beam position	Resolution
Setup A (297 MHz)	1.5 mm	3.66	0.89 nC	0.11 mm	$4.07 \mu\text{m}$
Setup B (297 MHz)	1.5 mm	4.26	0.88 nC	0.18 mm	$4.31 \mu\text{m}$
Setup C (60 MHz)	1.0 mm	2.46	0.88 nC	0.02 mm	$2.81 \mu\text{m}$

Although the dynamic range is relatively constrained (around 1.5 mm across all configurations) –likely due to

electronic saturation currently under investigation– the system exhibited high linearity, with χ^2 values near unity for the linear fits. The best resolution performance (Fig. 4), were achieved for an optimal bunch charge of approximately 0.88 nC/bunch and a beam positioned near the electrical center of the cBPM.

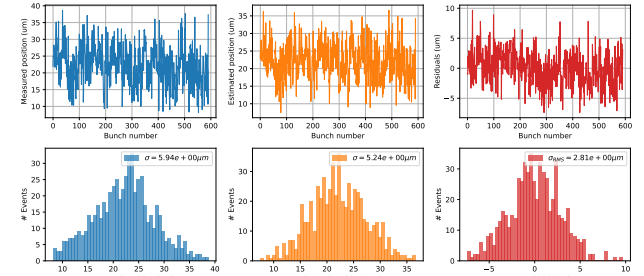


Figure 4: Peak resolution result obtained for the vertical plane using Setup C.

CONCLUSION

A synchronized analog down-conversion system for a cavity BPM has been successfully developed and validated through beam tests at the ATF. Iterative hardware enhancements optimized the LO synchronization, signal stability, and filtering performance.

Significant progress was achieved in the vertical plane, where the measured resolution was improved from $13.4 \mu\text{m}$ during the initial campaign to a peak value of $2.81 \mu\text{m}$ using a dual-stage down-conversion to a 60 MHz IF. These results demonstrate that utilizing lower IF can significantly enhance digitization quality, provided that sufficient waveform cycles remain available for accurate digital demodulation.

The results validate the proposed architecture and demonstrate its suitability for future FPGA+ADC real-time beam instrumentation systems. The deployment of a fully integrated ADC system is planned for late 2026 or early 2027, enabling a direct comparison between oscilloscope-based acquisition and fully integrated ADC systems, as well as the deployment of FPGA-based real-time digital signal processing.

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