PLANNED UPGRADE OF THE CERN PROTON SYNCHROTRON BEAM CONTROL SYSTEM

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Abstract

The CERN Proton Synchrotron (PS) Low Level RF (LLRF) system is composed of cavity controllers, which regulate the field in the cavities, and a beam control, in charge of maintaining the required longitudinal beam specifications and managing the injection and extraction processes. The current beam control system, implemented using mainly analogue electronics in NIM and VME formats, is set to be replaced by modern digital platforms that have been deployed on other machines in the complex. This upgrade aims for a redesigned, more centralized and standardized system. The new compact digital module will result in significantly reduced hardware requirements and improvement in diagnostics and maintenance. This paper provides an overview of the system's architecture, hardware, firmware, and development plan, focusing on the control loops and the interaction between the module and other components in the system.

MOTIVATION

since 1959, the PS has undergone numerous upgrades to supply proton and heavy ion beams, operating with charges between 10^8 and 4×10^{13} and reaching energies up to 26 GeV. The 628 m circumference ring features 25 RF cavities driven by six distinct RF systems spanning a frequency range of 0.4 to 200 MHz.

The LLRF architecture consists of two primary subsystems: cavity controllers and the beam control. The cavity controllers utilize single and multi-harmonic feedback loops to regulate the phase and amplitude of the RF signals delivered to the cavities. Meanwhile, the beam control subsystem employs radial, phase, and synchronization loops to maintain strict beam parameters and to coordinate injection and extraction timing with adjacent machines.

A renovation of the beam control system is currently underway (Fig. 1). The upgraded architecture utilizes two VMEbus Switched Serial (VXS) crates for the digital demodulation of beam loop inputs, alongside a microTCA crate that processes the beam loops [1]. This hardware selection aligns with CERN's broader strategy to standardize and improve existing accelerator technologies (LHC Injectors Upgrade project). Consequently, the VXS platforms mirror those already deployed in the PSB, AD, ELENA, and LEIR, while the beam loop architecture is based on the modernized systems of the SPS [2] and LHC.

The purpose of this new beam control is to implement the current analogue feedback algorithms as accurately as possible, but improving on diagnostics, operability and maintainability. The possibility of future feature addition is also to be kept in mind.

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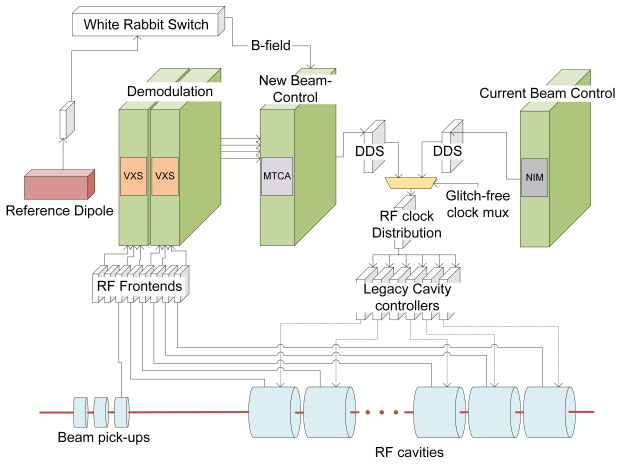

Figure 1: PS LLRF system diagram.

BEAM CONTROL ARCHITECTURE

Following the success in the deployment on the SPS and LHC, the PS Beam Control (Fig. 2) adheres to the same principle for firmware/software boundary definition in the FPGAs.

IP modules developed for other machines will be implemented in hardware for tasks like board housekeeping, White Rabbit (WR) Tx/Rx, generation of local timing from general machine signals, amongst others.

Some firmware modules were also developed for PS specific functions and where interaction with legacy systems was needed, such as the VXS acquisition.

A C++ application is in production for higher-complexity and higher-iteration parts of the beam control, such as calculation of the revolution frequency from the magnetic field [3] and the phase, radial, and synchronization loops.

HARDWARE

One of the main advantages of the new beam control is hardware standarization and condensation. Tens of racks, each having a few NIM crates populated with locally developed analogue electronics, are set to be replaced with two VXS crates and one microTCA crate. Each of the VXS crates contains two VXS switches and four VXS-DSP-FMC carrier boards, each containing two 4-channel 125 MSPS ADC FMCs. The carrier boards contain two FPGAs; one to demodulate and process the signals acquired through the two FMCs ADCs, and the other containg the signal acquisition core, function generators, timings and the so-called

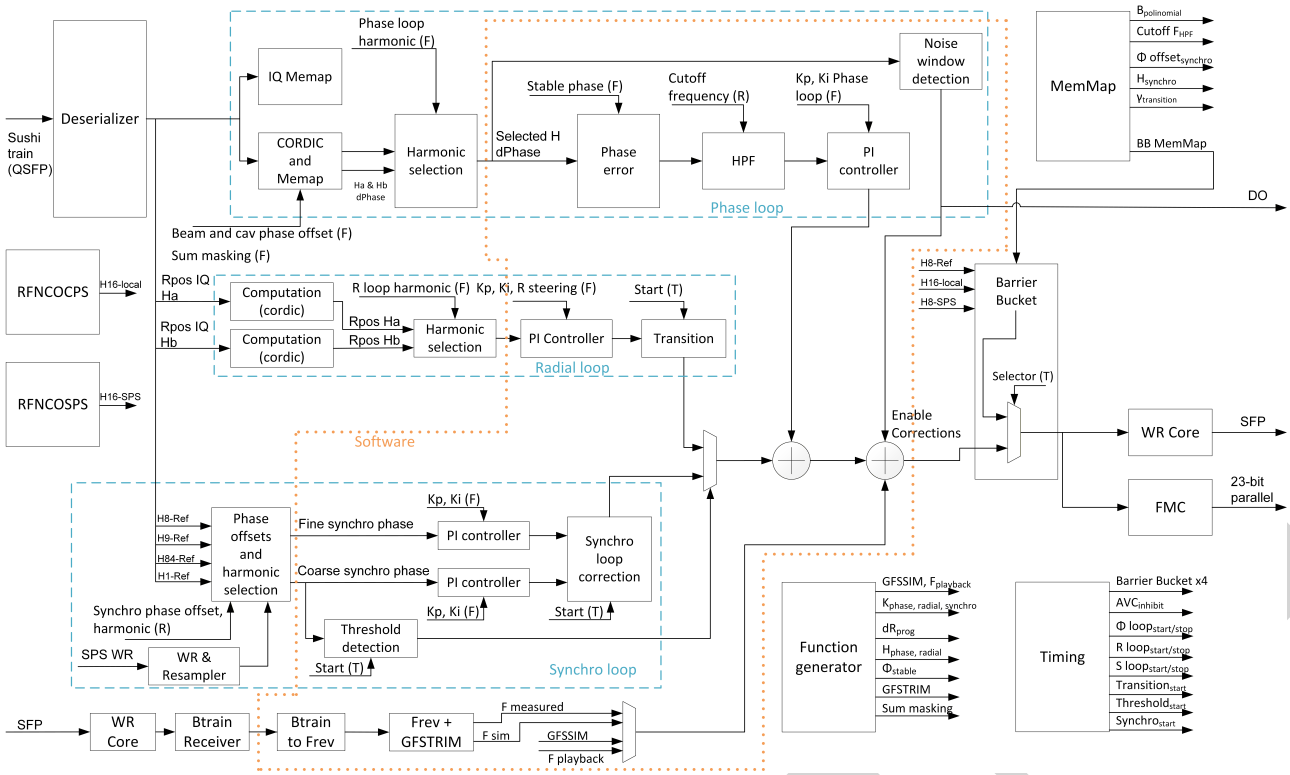

Figure 2: Beam Control block diagram.

VXS sushi-train for distributing the data across the VXS backplane to the VXS switches.

The microTCA crate includes a Central Timing Receiver AMC (CTRA) which interfaces to the CERN General Machine Timing system and an AFCZ dual FMC carrier board with Ultrascale+™ MPSoC, ultilising FPGA fabric and Arm CPU cores. The AFCZ FMC carrier has a Rear Transition Module (RTM) with SFP and QSFP ports, used to receive the IQ pairs from the VXS switch and the WR connection via optical fibres, and a 32 Ch DIO FMC for Frequency Tuning Word transmission (FTW) to the existing beam control's master DDS for beam synchronous clock distribution. (Fig. 3).

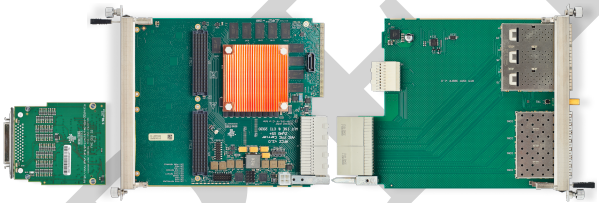

Figure 3: Beam-Control hardware, from left to right, the FMC, the AFCZ carrier and the QSFP-SFP RTM.

A downstream glitch-free clock mux allows to select on each cycle whether the current or new beam control is operational. This allows to run Machine Development tests in parallel to normal operation. This distribution scheme is set to be exchanged for a WR node (Fig. 4) should the latency budget for the loops allow it.

This setup would allow the PS to follow the standardization of FTW distribution seen in other machines. This,

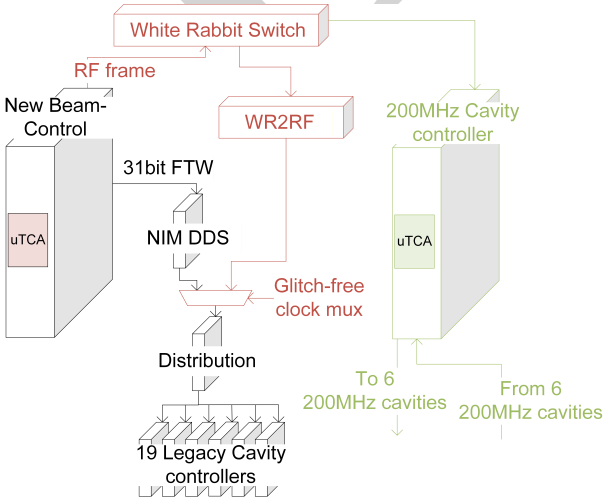

Figure 4: Layout of proposed WR distribution.

in turn, means that work can begin on the next proposed upgrade for the PS LLRF system: update of the 200 MHz cavity controllers based on the SPS C200 cavity loops [4].

TESTING PLAN

The upgrade of the PS Beam Control system faces a critical milestone in view of CERN Long Shutdown 3 (LS3), scheduled from September 2026 to July 2028. The extent to which the new system can be validated prior to this period will determine its readiness to replace the existing beam control and allow for its decommissioning during the shutdown.

For this, an incremental approach has been chosen to reduce risk and progressively implement and test each part of

the new beam control. The first test, for which machine installation is near completion, will focus on the IPs inherited from the SPS and LHC beam controls, as well as testing a firmware implementation of the Barrier Bucket module [5]. A prototype of this module is currently implemented on a microcontroller-based system, providing a functional reference for direct comparison, albeit with known reliability limitations. The transition to a dedicated hardware implementation is expected to address these issues, while enabling validation of the firmware functionality. These tests also constitute an initial verification of the system infrastructure, signal chain, and overall integration.

Following the validation of common services and housekeeping functionalities, the loops themselves will be tested. The phase loop will be addressed first, including verification of pre-injection locking, stable acceleration, and operation with multiple harmonics.

Subsequently, the radial loop will be commissioned, with emphasis on closed-loop operation in conjunction with the phase loop, as well as on its performance during transition crossing, for which it is required.

Finally, the synchro loop will be validated, including the handover from radial loop to synchro loop control. Here, radial steering is used to implement a beat frequency between the internal PS revolution frequency and the downstream machine (acting as the external synchronization reference), and subsequently the syncro loop is activated to bring the PS to the same frequency as the external reference.

Each control loop comprises both firmware and software components, the latter enabling rapid iteration and optimization during the testing phase. This staged approach ensures systematic validation of individual functionalities while progressively increasing system complexity.

CONTROLS

To configure the hardware for different accelerating cycles and beam configurations, settings are managed through the Front-End Software Architecture (FESA) and the LHC Software Architecture (LSA), which are deployed across the CERN accelerator complex. The settings and functions (i.e. parameters varying during the cycle) are generated either from conditional logic or computed from higher-level physics quantities such as momentum and bucket area. While this automatic generation framework is already established in machines such as the SPS and the LHC, its implementation for the PS remains incomplete and will be progressively developed and finalised during LS3. All settings are archived to enable configuration tracking, analysis, and rollback. For remote observation and diagnostics, several megabytes of bunch-by-bunch and turn-by-turn data are acquired on a per-cycle basis.

CONCLUSION

The development of the new PS Beam Control system represents a transition from analogue to fully digital implementation, with the objective of enhancing diagnostic capabilities and system maintainability. As one of the most significant upgrades to the LLRF system in the last decades, this evolution introduces non-trivial technical challenges, which are being addressed through iterative design and validation. Although the project timeline is constrained by the available shutdown period, progress is supported by the reuse of proven modules from other CERN systems and by parallel hardware and software development and testing activities, making the overall schedule achievable.

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