

# HIGH POWER GaN AMPLIFIER DEVELOPMENT FOR COUPLED-CAVITY LINAC AT LANSCE\*

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## Abstract

The Los Alamos Neutron Science Center (LANSCE) uses a coupled-cavity linac (CCL) to accelerate H<sup>-</sup> ions from 100 to 800 MeV. It is powered by forty-four 1.25 MW 805 MHz klystrons, each capable of 150 kW of average power. A prototype solid-state amplifier (SSA) that meets these requirements is in development. Commercial silicon LDMOS transistors have reduced power above 600 MHz and are also limited by the maximum drain to source breakdown voltage. We are using high voltage Gallium Nitride (GaN) on Silicon Carbide (SiC) high electron mobility transistors (HEMT) to reduce the number of active devices and the complexity of power combining smaller amplifiers. These wide bandgap semiconductors can operate at high channel temperatures around 200 degrees Celsius without shortened life. We are testing new devices up to 5 kW of peak power at 100 volts. Operating in saturation mode, out-phasing modulation is used to maintain high device efficiency to reduce thermal dissipation, compared to conventional class AB linear amplifiers. The power supply requires stored energy with a capacitor bank. Power combining uses a combination of 2-way Gysel, 40-way radial and magic tee combiners in waveguide.

## INTRODUCTION

The LANSCE facility uses a room-temperature copper CCL to accelerate H<sup>-</sup> ion beam from 100 to 800 MeV. This structure is powered by forty-four 1.25 MW 805 MHz klystrons, which all together provide approximately 44 MW of peak RF power and 5.3 MW of average power. These klystrons have been manufactured essentially unchanged since their introduction in 1968. LANSCE is expected to provide beams beyond 2050, which has raised concerns about relying solely on this vacuum electron tube technology for 24 years or more.

The LANSCE klystrons require 86 kV beam voltage supplied from conventional AC mains charging power supplies and capacitor banks, which present their own set of difficulties. The magnetic components (transformer and regulator) are no longer available from the original source. Seven capacitor banks, each feeding 6-7 klystrons, rely on

a large number of oil-paper insulated series/parallel capacitor strings. It is common for component failures to result in collateral damage in the bank due to the 230 kJ of stored energy. These high voltage equipment challenges are exacerbated as we add a younger engineering team less familiar with high voltage engineering than the designers who built the systems 54 years ago.

This institutionally funded R&D has been underway since 2024, to develop a replacement RF power amplifier that can fit in the space of one klystron and its modulator tank [1, 2]. Three-hundred and twenty solid-state amplifier (SSA) pallets are to be combined to produce equivalent or better performance than that of a klystron. This can replace the legacy high voltage vacuum electron tube technology with state-of-the art low voltage RF amplifiers. As an added benefit, this development has attracted and hired early-career engineers to help us form a strong R&D team.

## SSA DESIGN CONSIDERATIONS

### *Applicable Transistor Technologies*

Peak power capability has been a hallmark for vacuum tubes, where the thermal mass is large and the peak to average power ratio is very high. For a SSA, the most reliable approach is operating in continuous mode, and this has enabled silicon laterally diffused metal-oxide semiconductor (LDMOS) transistors to be combined to replace klystrons or inductive output tubes at dozens of synchrotrons and storage rings worldwide. Pulsed operation at the LANSCE CCL requires understanding the intrinsic peak capability of the individual junctions or channels inside the devices, their packaging for thermal design, and using energy storage with capacitors at one thousandth of the voltage of klystrons. Lessons learned from published SSA developments and discussions with staff from other accelerators using LDMOS were reviewed for this project.

LDMOS has been a mature technology from multiple manufacturers since 1990s, used for wireless communication, military, industrial and broadcast transmission. Transistors are made from large wafers in conventional silicon foundries so the price per watt is attractive. Rated at a maximum operating  $V_{ds}$  (drain to source) voltage of 50-65 volts these field-effect transistors generate up to 1.9 kW of saturated peak power below 400 MHz. A recent exception is a 4 kW peak LDMOS device operating at 75 Volts up to 450 MHz. At 805 MHz the peak power capability is reduced significantly. The drain to source capacitance of large LDMOS devices limit their maximum frequency-times-power product. Conventional linear amplification

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(class AB) requires back off of the power from the saturated datasheet value,  $P_{\text{sat}}$ , which is measured with a specific amount of gain compression. This reduces the desired power capability to below 1 kW in the ultra-high frequency (UHF) band.

There are an increasing number of applications at UHF to low microwave ranges that are moving to wide bandgap semiconductors such as GaN. The bandgap is 3.4 eV compared to 1.1 eV for LDMOS. As a result, the breakdown field in the device is 2 MV/cm whereas in LDMOS it is  $\sim 300$  kV/cm. Output shunt capacitance ( $C_{\text{ds}}$ ) is  $\sim 1/4$  that of LDMOS and input capacitance ( $C_{\text{gs}}$ ) is 50% less. Power density is 5-20 W/mm of gate periphery for HV GaN and 2 W/mm for 50 volt LDMOS. By adjusting the doping and gate field plate design, GaN on SiC HEMT have been developed for 150 volt drain to source voltage ( $V_{\text{ds}}$ ) at UHF to L band frequencies [3, 4]. Impedance matching from the drain tab to 50 ohm loads is improved with higher drain voltage, as determined by this relationship:

$$\text{Optimal load resistance, } R = \frac{(V_{\text{ds}} - V_{\text{sat}})^2}{2 \cdot P_{\text{out}}} \quad (1)$$

where  $V_{\text{sat}}$  is approximately 10 volts for GaN HEMT. The number of components and size of the output circuit is reduced when drain load is closer to 50 ohms.

The pallet is a functional block of HEMT plus passive matching circuits and DC bias networks. A pair of pallets is combined to make a 10 kW blade, which has a local protection and communication board, gate bias sequencer with drain overcurrent sensors, and puck circulators for each pallet. Forty blades are summed together in a radial power combiner to reach 350 kW,  $1/4$  of the total power of the entire SSA.

We have evaluated push-pull 3.6 kW HEMTs from a transistor fab with HV GaN on SiC optimized for pulsed RF power. The IGN815 device uses conventional Ag-Sn die attach in a Gemini package and is designed for 12% duty factor (Fig. 1). A 5 kW pallet was designed using a pair of new IGN825 single-ended HEMTs, combined on the pallet (Fig. 2). This is the final configuration that will be used for the LANSCE power amplifier.

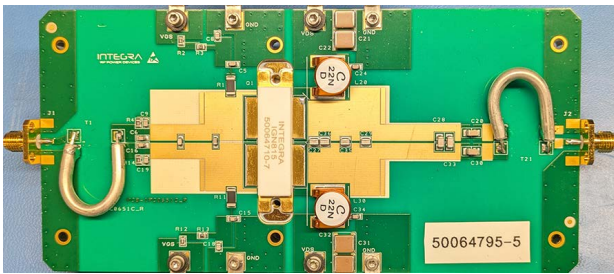


Figure 1: 3.6 kW pallet using IGN815 HEMT.

Our SSA lab is equipped with pallets on water-cooled plates, RF source, driver amplifier and loads, and a high-current power supply along with local electrolytic capacitors. We are testing 16 pallets for repeatability of power, gain, efficiency, phase response, all with varying duty

factors and temperatures [5]. Table 1 shows measured data from both types of HEMTs.

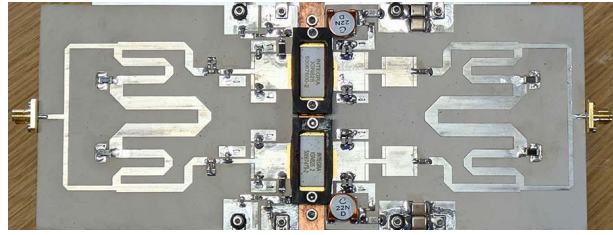


Figure 2: 5 kW Pallet using IGN825 HEMTs.

Table 1: Comparison of Two HEMT Pallets

805 MHz 1mS PW, 120 pps	IGN815	IGN825
$V_{\text{ds}}$ (DC)	100	100
$P_{\text{out}}$ (W)	3600	4659
Gain (dB)	19.2	18.1
DC/RF (%)	71.5	68.5
Efficiency		

### Thermal Considerations

Like the klystrons that it could replace, the SSA will require a similar amount water cooling, through cooling plates with many flow and temperature interlocks. This is a design space that heavily impacts the piping layout as well as the instrumentation and control design. In silicon LDMOS it is typical to operate the semiconductor at 150 – 170 degrees C. GaN on SiC, on the other hand, can operate with channel temperatures higher than 200 deg C. Arrhenius plots suggest one million hours is achievable at 225 °C [6]. It has been especially important to work with the HEMT manufacturer using their thermal parameters measured using advanced techniques [7]. The balance of circuitry of the overall system should set the limit for SSA mean time to repair, and this analysis is ongoing.

### Outphasing Modulation Method

Linear class AB amplification implies peak power operation below  $P_{\text{sat}}$ . Operating at reduced power with high drain voltage raises the drain power dissipation as the efficiency is lower with this poorly matched loadline (eq. 1). In the selected HEMT, high peak power and 12% duty factor results in  $\sim 260$  watts of average power that will be dissipated at full power. This will increase as drive power is reduced. Unlike a klystron that dumps power into a massive collector regardless of RF drive, GaN HEMTs must consider specific situations:

- When conditioning a CCL cavity
- Ramping up power slowly to minimize sparking
- During accelerator beam tuning
- Normal uneven RF power distribution along linac
- Fast power fluctuation for beam loading

The outphasing modulation technique of Chireix has been resurrected from historic tube use [8, 9]. Fundamentally, it uses a pair of identical amplifiers operating at maximum (saturated) efficiency. Linear amplitude modulation is then obtained using nonlinear amplifiers operating with varying phase-relationships prior to recombination. This PM to AM modulation prevents the HEMT from operating at low efficiency at any time. Figure 3 illustrates the general concept. This scheme doesn't come without another problem. Reflected power back to each PA varies with the phasing, being highest when both amplifiers are at 180 degrees opposition. Circulators and magic-tee waveguide combiners are used in the SSA, and the amount of outphasing is restricted by design.

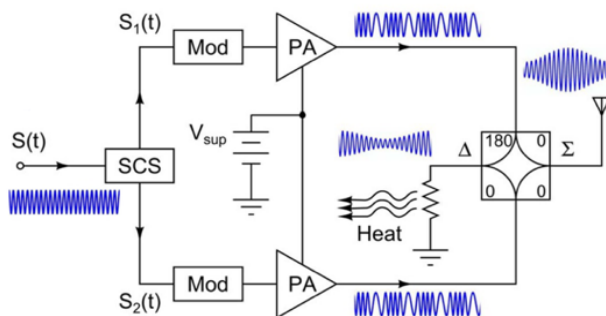


Figure 3: Outphasing Amplifier (adopted from Godoy, IEEE Trans MTT, Dec. 2009).

Outphasing modulation for amplitude control is developed in the digital low level RF controller [10-12]. Phase modulation for the overall SSA is developed with conventional PI feedback loop outside of the outphasing system. 14 dB (50-1250 kW) of controlled dynamic range is required, where faster outphasing will be used for amplitude feedback for beam loading compensation and pulse-flattening while slower power reduction via switching off designated pallets will handle larger power adjustments needed. RF modelling is underway to determine the impact of shutting off selected pallets to accommodate these power reductions that are not handled with outphasing.

### Combined Pallets

For a SSA with 320 RF pallets, combining networks must have low loss and the highest number of combined blades to be most efficient. The limiting power level of a blade is 10 kW peak and 1.2 kW average, determined by the coaxial RF connector, a modified 7/16 DIN type. A radial waveguide combiner with 40 input ports and waveguide flange for output is being fabricated by a passive RF components manufacturer. Two of these will be powered back-to-back with 40 phase matched cables using a klystron as a power source, to test the combiner peak and average ratings. This experiment will be conducted at the SNS klystron test facility at Oak Ridge National Laboratory. A matching 40-way splitter to drive the blades is also in development. This 1/4 module generates 350 kW peak power with 40 blades. It is combined with three others using waveguide magic tees to the final combination for 1.25 MW (Fig. 4). One high power circulator will be

between the final magic tee and the CCL, similar to what a high efficiency klystron requires. Testing of passive components for the complete combining network has been described previously [13]. Measurements have characterized 5 kW circulators from various manufacturers over elevated temperatures and with proximity to each other (stray magnetic field), in search for the best devices for this SSA.

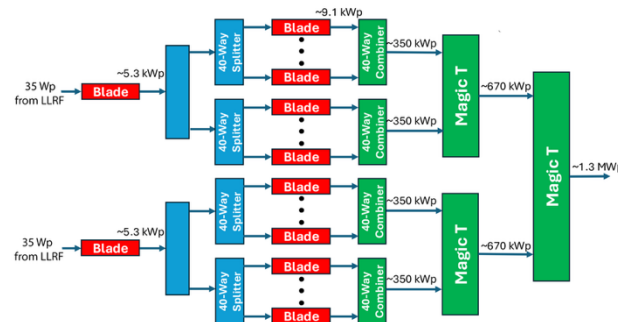


Figure 4: Overall power amplifier architecture.

### AC/DC Power

As the SSA is a pulsed load, DC power must have sufficient stored energy for pulse flatness and to avoid significant flicker on the AC power network. We are studying the optimal location of this storage, likely to be a combination of bulk capacitance at the converters as well as distributed capacitance closer to the pallets. The exiting AC grid supplies 4.16 kV AC to the mains power supply for LANSCE klystrons. This would be reconfigured to accommodate switch-mode power converters with 480 V mains voltage. Work is ongoing to define the optimal capacitors values and types to store energy.

### CONCLUSION

A new SSA is being developed to supplant 805 MHz high power klystrons at LANSCE. Various trade studies are underway for the engineering details of the amplifier. Prototype GaN on SiC HEMT are being tested, and plans for the remaining year include testing higher power combinations to test effectiveness of outphasing modulation. Leading-edge technologies are being used to overcome shortcomings that would otherwise make a 1.25 MW pulsed SSA at 805 MHz very complex, physically large and inefficient. GaN on SiC devices allow us to design a more compact SSA that will not become obsolete within a few decades.

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