

R&D ACTIVITIES IN VIEW OF PIP-II LB650 CAVITY PRODUCTION

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Abstract

A joint LASA–Fermilab activity is in progress to study the impact of key surface processing steps on the performance of LB650 superconducting cavities in view of future series production. Among the several cavity preparation steps, electropolishing (EP) and mid-temperature heat treatment are considered the most critical and require specific optimization for the LB650 geometry. Single-cell and 5-cell cavities are used as test prototypes to investigate the effects of EP and mid-temperature bake. Vertical RF tests are performed at Fermilab after EP and after the mid-T bake under identical conditions. The ongoing program aims to provide insight into the evolution of Q_0 and accelerating gradient along the processing sequence. Preliminary observations and results are here presented.

INTRODUCTION

LASA-INFN is responsible for the production and qualification of the low-beta cavities for the PIP-II Project. The low-beta section is a key part of the PIP-II superconducting linac, accelerating the H^- beam from approximately 177 MeV up to 516 MeV before injection into the downstream high-beta section. It consists of 36 five-cell elliptical superconducting cavities (labeled in the following as LB650), operating at a frequency of $f = 650$ MHz and designed for a geometric beta factor of $\beta_g = 0.61$ [1]. The project specifications for the LB650 cavity operation in the linac are an accelerating gradient of $E_{acc} = 16.9$ MV m⁻¹ and an intrinsic quality factor of $Q_0 = 2.4 \times 10^{10}$. To ensure an adequate performance margin, the acceptance criterion in the vertical test of the naked cavity is set to a higher value, corresponding to at least $Q_0 = 2.9 \times 10^{10}$ at nominal field. This vertical test performance therefore represents the effective qualification target for cavity acceptance and subsequent cryomodule integration. Given the demanding quality-factor requirement, the choice of an appropriate surface treatment is crucial [2]. Following an extensive R&D campaign carried out on single-cell and multi-cell cavity prototypes, a recipe based on medium-temperature furnace baking was selected. Compared to other high- Q_0 treatments, such as nitrogen doping, mid-temperature baking offers a simpler and more robust process chain for the LB650 cavity geometry, as it does not require an additional electropolishing step to optimize the impurity diffusion profile in the RF penetration

layer. Among the various temperature-time combinations investigated by the SRF community, a treatment at 350 °C for 3 h was selected as the baseline recipe. This choice results from the favorable balance between BCS resistance reduction and magnetic flux sensitivity, while preserving compatibility with the cavity geometry and industrial processing workflow. Studies on 650 MHz cavities have shown that medium-temperature baking in this temperature range can provide quality factors comparable to nitrogen-doped cavities, while significantly simplifying the final surface preparation procedure [3].

SURFACE PROCESSING OPTIMIZATION

To support the industrial implementation of the medium-temperature baking treatment for the PIP-II LB650 cavity production, a dedicated investigation was established to assess the reproducibility and consistency of the surface preparation workflow implemented by the qualified vendor. This activity was conceived as a process verification strategy aimed at consolidating the treatment recipe under production-relevant conditions, with particular focus on the electropolishing (EP) and furnace baking stages. The objective of the campaign was to verify that both the EP infrastructure and the furnace treatment could reproduce performance levels consistent with those previously observed during the R&D phase on prototype cavities. To this end, historical vertical test data collected on comparable cavities under similar operating conditions were used as reference guidelines to frame the expected performance and support the interpretation of the experimental results. To this purpose, two configurations were selected. The first one was the INFN single-cell prototype cavity EZ-SCCFG004, developed within the PIP-II R&D program and fully representative of the reference cavity geometry. The second was the five-cell 644 MHz elliptical cavity S65-001, owned by Michigan State University and designed for the FRIB energy upgrade [4], which was selected as a multicell benchmark. Although not a nominal PIP-II LB650 cavity, S65-001 features comparable geometrical and RF characteristics, thus providing a structure of similar complexity and dimensions for validating the industrial workflow. Both cavities were tested in two different surface conditions: after the *Baseline EP* process and after the application of the *Medium-Temperature Baking* treatment at 350 °C for 3 h. This approach enables a direct comparison of the RF performance before and after the furnace treatment, allowing the assessment of both the treatment

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effectiveness and the reproducibility of the complete industrial process. The main performance indicator considered in this campaign was the intrinsic quality factor, Q_0 , measured at the nominal operating gradient ($E_{acc} = 16.9 \text{ MV m}^{-1}$). The reference values reported in Table 1 were derived from historical vertical test measurements of prototype cavities processed under comparable conditions and are used here as practical benchmarks for the evaluation of the measured performance. In particular, the reference thresholds correspond to the lower bound of the historically observed performance range, while the average values achieved under the same treatment conditions is also reported for comparison.

Table 1: Reference guidelines for this study. EP refers to the baseline electropolishing treatment, while Mid-T indicates the medium-temperature baking treatment

Cavity-Step	Ref. Q_0	Avg. Q_0
EZ-SCCFG004-EP	2.40×10^{10}	3.54×10^{10}
EZ-SCCFG004-Mid-T	3.35×10^{10}	4.84×10^{10}
S65-001-EP	2.18×10^{10}	3.22×10^{10}
S65-001-Mid-T	3.05×10^{10}	4.40×10^{10}

Cavity Surface Treatments

All the surface treatments reported in this work were performed at Zanon Research & Innovation Srl (ZRI), the industry responsible for the manufacturing and surface treatment of the PIP-II LB650 series cavities. ZRI has also produced and qualified several prototypes cavities for Fermilab and INFN. Building on the experience gained during these previous activities, both the infrastructure and the treatment protocols have been significantly optimized [5]. Figure 1 shows representative views of the two main infrastructures employed in this study, namely the Electropolishing (EP) plant and the furnace for mid-T baking.

Baseline EP The EP plant has been adapted to the LB650 cavity geometry by increasing the cathode surface, reducing the cavity-to-cathode surface ratio from the original 10:1 to 5:1. This modification increases the current density at the equator region, thereby enhancing the local material removal rate and the corresponding surface smoothing effect. For both “warm” and “cold” EP treatments, the optimal operating voltage is determined for each process through the acquisition of the I–V polarization curve, allowing the working point to be set at the center of the polishing plateau.

Overall, the treatment sequence for the baseline EP condition consists of:

- A bulk EP removal aimed at fully resetting the initial surface condition, consisting of an extended “warm” EP (80 μm for cavity EZ-SCCFG004 and 100 μm for cavity S65-001), followed by a 20 μm cold EP;
- A high-temperature annealing treatment under ultra-high vacuum, consisting of 3 h at 900 °C;
- A final EP removal, consisting of a 20 μm “warm” EP followed by a 20 μm “cold” EP.

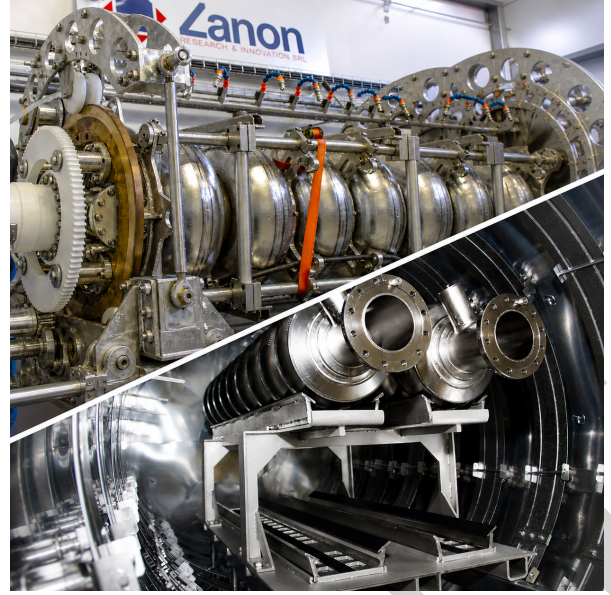


Figure 1: Representative views of the electropolishing (top) and vacuum heat-treatment furnace (bottom) facilities used for the study.

Medium-temperature baking The furnace employed is the same used for the other high temperature processes. Therefore, in order to ensure an adequate level of cleanliness and purity, a high-temperature annealing cycle of the empty furnace is performed before each mid-T cycle. After the baseline EP, the cavity is transferred to the clean room where, following High-Pressure Rinsing (HPR), it undergoes a 48 h air exposure in an ISO4 environment to allow for stable reoxidation of the niobium surface. The cavity is then loaded into the furnace. The thermal cycle consists of a linear heating ramp from room temperature up to the process setpoint, followed by a 3 h dwell at 350 °C. At the end of the medium-temperature bake, the cavity is allowed to cool down naturally by switching off the heating system. Once extracted from the furnace, the cavity is transferred back to the clean room for the final cleaning procedures and preparation for the subsequent vertical test.

EXPERIMENTAL RESULTS

All RF tests presented in this work were performed at Fermilab using the Vertical Test Facility (VTS), in order to ensure measurement consistency and to minimize systematic uncertainties associated with different test infrastructures. In particular, great care was taken to reduce the contribution of the residual resistance associated with trapped magnetic flux during cooldown, which is particularly critical for mid-T treated cavities [6]. For this reason, all tests were performed under active magnetic field cancellation using external Helmholtz coils. In the case of single-cell cavities, a single coil system is sufficient to achieve an almost complete field compensation at the cavity equator. For multicell cavities, instead, two independent coil systems were employed. Although a perfect cancellation of the ambient field along the full cavity length is not achievable, the magnetic field in

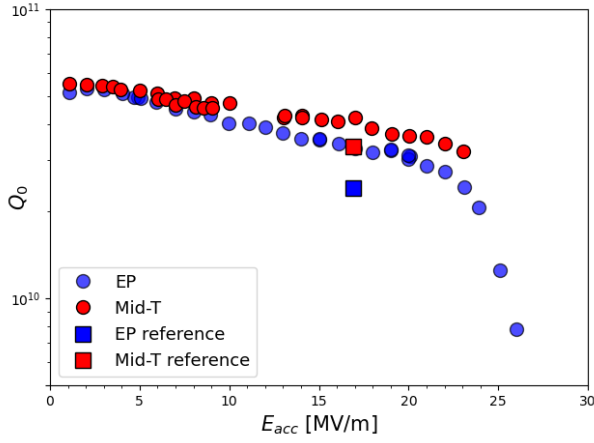


Figure 2: RF cold test results for single cell EZ-SCCFG00.

the RF region is typically reduced below 0.2 mG. In addition, a standard fast cooldown procedure was applied in all measurements. This approach promotes efficient magnetic flux expulsion from the superconducting niobium surface, further reducing trapped flux contributions to the residual resistance.

Single Cell EZ-SCCFG004

The results of the two vertical tests of cavity EZ-SCCFG004 after EP and after mid-T at 2 K are reported in Fig. 2. A first test performed after the mid-T baking is not shown, as it was affected by strong field emission (FE) and therefore did not allow a reliable evaluation of the cavity performance. The cavity was subsequently re-tested after an additional HPR, which led to a substantial reduction of the FE activity, although a residual contribution was still present without significantly affecting the cavity performance. While the low-field Q_0 values measured in the two tests are comparable, a more pronounced high-field Q-slope is observed for the baseline EP condition, as expected due to the absence of a final baking treatment, which is known to mitigate this effect [7]. Overall, the measured Q_0 values at the nominal operating gradient are 3.3×10^{10} and 4.2×10^{10} for the baseline EP and mid-T baked conditions, respectively, both exceeding the reference values reported in Table 1. In particular, the baseline EP result proved to be significantly higher than expected. This exceptionally high performance partially reduces the gain provided by the mid-T baking, whose improvement at the operating gradient is less than 30% with respect to the baseline EP condition.

Multicell S65-001

The results of the two vertical RF tests of cavity S65-001 at 2 K are reported in Fig. 3. The measured Q_0 at the nominal operating gradient for the baseline EP condition is 2.8×10^{10} , in good agreement with previous results obtained using a similar recipe [8]. After the mid-T bake, the Q_0 increases to 4.1×10^{10} . In both cases, the measured values exceed the historical reference levels reported in Table 1. A reduction in the maximum E_{acc} with respect to the baseline EP condition

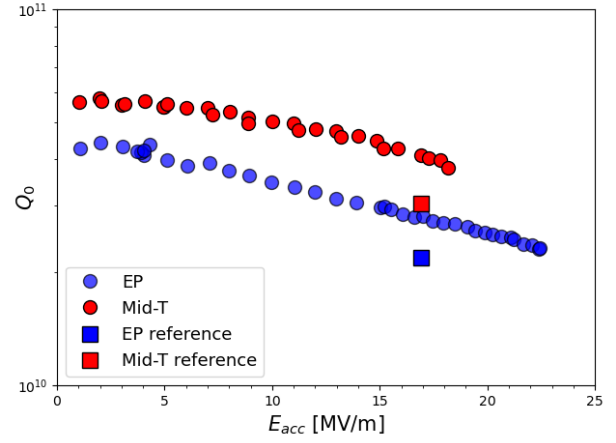


Figure 3: RF cold test results for multicell S65-001.

is also observed, with a lower quench field in the high-field regime. This behaviour is consistent with trends commonly reported for similar recipes [9]. Notably, the high initial Q_0 values and the significant enhancement at the operating gradient observed in both vertical RF tests demonstrate that performance levels typically achieved in dedicated R&D facilities can be reproduced also at the vendor level. The combined optimisation of the EP and mid-temperature (mid-T) processing steps thus leads to an overall improvement in the superconducting performance of the multicell cavity S65-001, with final results well above the reference baseline.

CONCLUSIONS

This paper reports the optimization campaign carried out in a joint effort between FNAL and INFN-LASA on two cavity prototypes representative of the forthcoming INFN series production of PIP-II LB650 cavities. The main objective was to explore the capabilities of the infrastructures and study the surface processing steps associated to the high- Q_0 treatment recipe based on medium-temperature baking. The results presented herein show that the industrial implementation of both the electropolishing and medium-temperature baking processes is feasible. In all investigated cases, the measured Q_0 values at the target gradient were found to be above the expected performance range. Although a reduction of the quench field after the medium-temperature baking treatment was observed in the multicell cavity, this behavior is consistent with observations commonly reported for this treatment. Overall, the present results support the implementation of the workflow in the industry even if further optimizations are required to apply it for the series production.

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