DEVELOPMENT OF A SIMULATOR FOR RING ACCELERATOR ELECTRON BEAM SIGNALS

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Abstract

Beam diagnostic systems are crucial for the Hefei Advanced Light Facility (HALF), a fourth-generation light source under construction. However, the testing of its key devices—such as Digital Beam Position Monitors (DBPMs), the Fast Orbit Feedback (FOFB) system, and Bunch-by-Bunch (BbB) processors—is limited by the lack of a laboratory signal generator capable of simulating accelerator physics, which hinders comprehensive closed-loop testing prior to installation. To address this, we have developed an FPGA-based hardware simulator featuring two input ports for feedback signals and four output ports with independently adjustable signal amplitudes and synchronous triggers. It integrates a simplified physics model to generate realistic, wideband beam signals with a pulse width of approximately 5 ns, enabling low-cost, repeatable testing without an actual beam. The system quantizes real bunch signals, simulates transverse/longitudinal oscillations in an FPGA, and outputs specific waveforms upon a set trigger. By modelling beam dynamics, it also produces signals closely resembling those expected during actual operation in Hefei Light Source (HLS). This simulator assists in designing and optimizing beam feedback algorithms while reducing development difficulty for DBPM and BbB systems. Crucially, it fulfills application needs by enabling previously impossible lab tests—such as evaluating BbB algorithms and measuring FOFB latency/bandwidth—before the beam is ready.

INTRODUCTION

As a fourth-generation diffraction-limited storage ring synchrotron light source, HALF is currently under construction [1]. The associated beam diagnostic devices are being developed to ensure the facility can produce bunches with low emittance, small size, and high brightness.

Under laboratory conditions, only simple single-item tests can be conducted on these systems and algorithms, such as single-frequency verification of DBPM performance, ADC sampling accuracy of feedback systems, and validity of data transmission logic [2-4]. Tests involving beam pattern dependence of measuring instruments and closed-loop characteristics of feedback systems require on-beam measurements inside the storage ring, together with specific bunch filling modes provided by accelerator facilities, which is extremely inefficient and inconvenient.

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To address this issue, a beam simulation algorithm is developed based on a four-output-port FPGA+DA hardware platform, supporting adjustable signal amplitude and synchronous triggering. As illustrated in Fig. 1, the designed system can generate realistic beam signals, enabling low-cost, repeatable device testing without actual beams, and facilitating offline optimization of feedback algorithms.

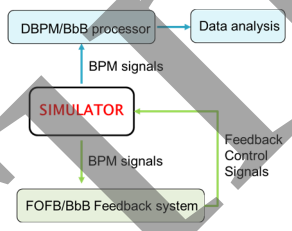

Figure 1: Schematic diagram of simulator application.

PHYSICAL PRINCIPLE

Generation of BPM Signals

Assuming a Gaussian charge distribution in the electron bunch, the induced voltage on button electrodes can be expressed as [5]:

$$V_B(t) = \frac{\pi a^2}{2\pi b}\frac{1}{\beta c}\cdot Z\cdot\frac{t-t_0}{\sigma^2}\cdot I(t)\cdot\frac{a^2-\delta^2}{a^2+\delta^2-2a\delta cos\theta}, \quad (1)$$

$$I(t) = \frac{Q}{\sqrt{2\pi}\sigma}e^{-\frac{(t-t_0)^2}{2\sigma^2}}. \quad (2)$$

Figure 2 shows the parameters involved, and Q is the bunch charge, σ is the bunch length, βc is the beam velocity, t_0 is the phase offset, and Z is the transfer impedance (mainly the equivalent impedance of the coupling capacitance between the electrode and the beam pipe wall as well as external cable impedance), and $I(t)$ represents instantaneous current of the bunch.

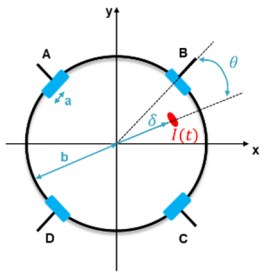

Figure 2: Beam parameters in the storage ring.

Transverse and Longitudinal Oscillations

In practical accelerator storage rings, the transverse and longitudinal positions of particle beams deviate from the

equilibrium orbit. The actual transverse beam position can be described as [6]:

$$x = x_\beta + x_\varepsilon + x_c\,, \tag{3}$$

$$y = y_\beta + y_c\,, \tag{4}$$

where $x/y_\beta(s) = a\sqrt{\beta_{x/y}(s)}\cos(\varphi_{x/y} + \varphi_0)$ are displacements due to beta oscillations, x_ε is the radial offset caused by energy dispersion, x/y_c are closed-orbit distortions due to magnet defects and tolerances. The Root-Mean-Square values of x and y characterize horizontal and vertical bunch sizes respectively.

Longitudinal beam position refers to the geometric or charge-weighted average of the bunch center projection along the beam direction, jointly determined by ring-wide longitudinal radio frequency fields, bunch energy spread, bunch phase, momentum compaction factor and fundamental RF frequency etc [6]. In actual measurement, the zero-crossing of the bunch signal is mainly used to characterize the longitudinal position.

Figure 3 illustrates Turn-by-Turn (TbT) transverse and longitudinal oscillations acquired by oscilloscope during normal operation of the Hefei Light Source. Once these data are obtained, they are quantized into four-channel amplitude modulation factors and phase shift data, stored in the FPGA, and then applied to adjust the signal accordingly before it is output to the DAC.

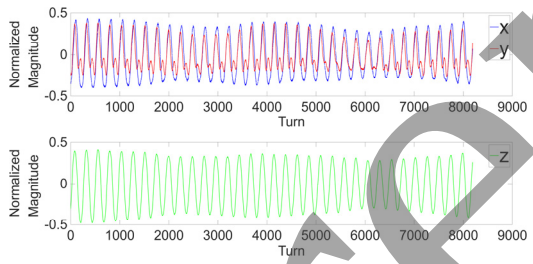

Figure 3: TbT transverse and longitudinal oscillations of HLS.

ALGORITHM ARCHITECTURE

Bunch-Location-to-Signal Algorithm

According to formula (1) and (2), beam signals can be calculated via analytical functions given known bunch parameters. Implementing this function in hardware code enables BPM signal generation.

Figure 4 illustrates the dataflow implemented on FPGA hardware for generating beam simulation parameters. Various input parameters (e.g., bunch charge, bunch length, time offsets etc.) are fed into several multipliers and dividers and a Floating-point IP core (configured to perform exponential operations). The outputs of these IP blocks are then aligned in parallel and sent to a multiplier. The three types of IP cores in the middle of the flow are all standard Vivado IP cores. This optimized pipeline enables real-time processing of BPM signals calculated from the position of the bunches.

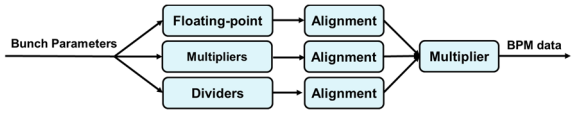

Figure 4: Bunch Location to Generate Signals Algorithm.

Oscillation Simulation Algorithm

At present, another algorithm shown in Fig. 5 is mainly used to generate beam signals. The overall algorithm flow is as follows:

- The beam signal is sampled by a high-sampling-rate oscilloscope, quantized into a 16-bit data array, and stored in the FPGA's ROM.

Considering that longitudinal oscillation is realized by adjusting the read start address of the data, special handling of the stored data length is required when quantizing the data. The number of points for a single period (2 ns) of the bunch signal is controlled to 2000 points, achieving a longitudinal adjustment accuracy of 1 ps.

- Adjust the amplitude modulation factor and phase shift for each channel of each bunch according to the transverse oscillation parameters.

Given the transverse oscillation parameters of the beam in the storage ring, the amplitude modulation factors for the four BPM signals can be calculated by inverse operation of the difference-over-sum algorithm as follows:

$$k_{A,B,C,D} = k(\pm x \pm y), \tag{5}$$

where k is a parameter related to the storage ring and pick-up structure.

The simulation of longitudinal oscillation is achieved by the "read address offset method". The original bunch waveform data is stored sequentially in ROM. During normal output, reading starts from address 0. To simulate a bunch arrival time advance by Δt, reading starts from address $\Delta t/t_s$ (where t_s is the sampling period); to simulate a delay, the address is postponed by the same amount. The address offset can be changed independently in each trigger cycle without regenerating waveform data, resulting in low resource consumption.

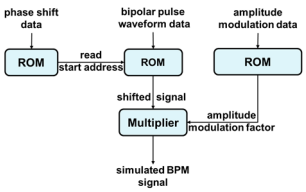

Figure 5: Oscillation Simulation Algorithm.

SIMULATION AND TEST

Pre-Simulation

Turn-by-turn Oscillation Simulation Pre-simulation verification of the beam simulation algorithm was completed on the Vivado platform. A single-trigger output mode of 16 bunches was used, with the transverse position of each bunch varying according to a preset oscillation curve. The simulation results illustrated in Fig. 6 that the modulated bunch amplitude changes with the trigger index.

Comparison of the exported FPGA simulation results with reference data shows consistency, verifying the correctness of the transverse oscillation logic.

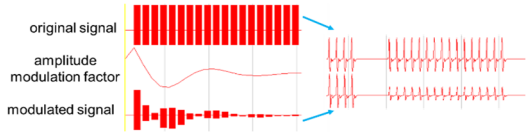

Figure 6: Simulation for the Transverse Oscillation Algorithm.

The simulation verification of longitudinal oscillation focuses on the control accuracy of the address offset. Configuring the ROM address offset to 50 (equivalent to 50 ps time shift), the simulation results (Fig. 7) show that the shifted waveform arrives 50 ps earlier than the reference waveform with no offset. By observing the timing relationship between the trigger signal and the output waveform, it is confirmed that the offset loading takes effect independently in each trigger cycle.

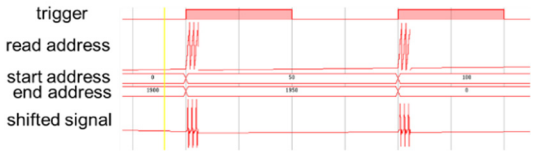

Figure 7: Simulation for the Longitudinal Oscillation Algorithm.

Four-channel Coefficient Joint Simulation Applying the transverse oscillation amplitude factors and longitudinal oscillation address offsets simultaneously to all four channels, the simulation outputs a set of four-channel waveforms containing 16 bunches. Figure 8 shows the transverse oscillation data used in the simulation and the calculated amplitude adjustment factors for each of the four channels. We select one of the amplification factors of one of the bunches for error analysis. Due to quantization error, at points where the original waveform data are small (i.e., DC data points), the amplification factor appears inconsistent. Considering that these points have little impact on waveform analysis, the transverse position sequence recovered from the amplitude values of the four channels can match the preset transverse oscillation curve. As shown in Fig. 8, the result verifies the correctness of the four-channel coupled output, proving that the simulation algorithm can generate beam signals that are consistent with the mathematical model of the real BPM signal oscillation.

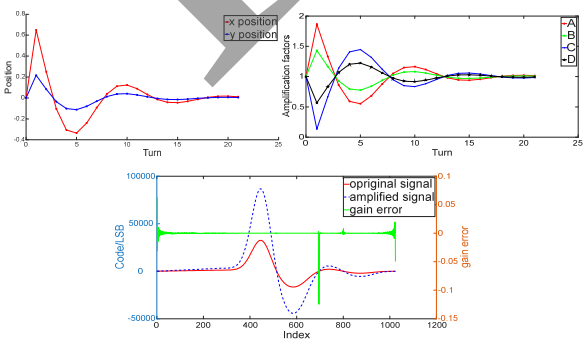

Figure 8: Simulation for four-channel coefficients.

Preliminary Laboratory Test

The logic correctness of the algorithm was tested on a custom-designed FPGA+DA board. Limited by the existing DAC with 1Gsps sampling rate, a continuous bunch signal at 204.03 MHz (Radio Frequency of HLS) with a peak-to-peak amplitude of approximately 450 mV (Fig. 9) was generated instead of 499.8 MHz (that of HALF).

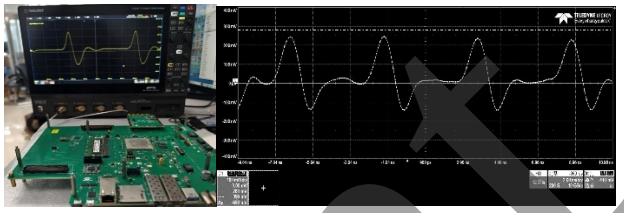

Figure 9: Test platform and preliminary test result.

CONCLUSION

In this paper, we have developed an FPGA-based beam signal simulator to address the lack of laboratory testing capabilities for beam diagnostic and feedback systems at HALF. Two algorithmic approaches were proposed: a real-time computation pipeline using Floating-point IP cores to derive BPM signals directly from bunch parameters, and a more resource-efficient method based on waveform ROM with dynamic amplitude scaling and read-address offset for simulating turn-by-turn oscillations.

The latter algorithm was implemented and verified on a Vivado platform. Pre-simulation results demonstrated that the simulator can output several consecutive bunches with both transverse and longitudinal oscillations under a single trigger, achieving a longitudinal time-shift precision of 50 ps. Four-channel coupled outputs were validated to be consistent with the mathematical model of beam oscillations. Preliminary laboratory tests using a 1Gsps DAC successfully generated a continuous bunch signal at 204.03 MHz with a peak-to-peak amplitude of approximately 450 mV, confirming the basic functionality of the algorithm.

The proposed simulator provides a low-cost, repeatable, and offline test for DBPMs, FOFB systems, and BbB processors, overcoming the limitations imposed by scarce beam time and enabling previously infeasible laboratory evaluations such as closed-loop feedback optimization and latency/bandwidth measurements. Future work will focus on implementing higher-speed DACs and RF amplifiers to achieve a wider range of amplitude adjustment for a 499.8 MHz output signal for HALF, supporting more filling patterns, and integrating ADC feedback to enable full closed-loop parameter optimization of the bunch-by-bunch feedback system.

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