INTEGRATING FPGA INTO EPICS FOR ON-THE-FLY SCAN CONTROL AT THE TPS 35A BEAMLINE

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Abstract

On-the-fly scanning is an effective technique for improving data-collection efficiency in X-ray Absorption Spectroscopy (XAS). Its application at undulator beamlines requires deterministic synchronization among undulator motion, beamline energy scanning, and data acquisition. To address these requirements, a hardware-integrated on-the-fly scan control system has been developed for the TPS 35A beamline, which is currently under construction.

The proposed system integrates a Field-Programmable Gate Array (FPGA) based hardware backend with the Experimental Physics and Industrial Control System (EPICS) control framework. EPICS provides supervisory beamline control, including scan configuration, operation flow management, and system monitoring, while all time-critical synchronization and processing are executed in FPGA hardware. In a fixed master–follower scheme, the EPU66S undulator gap motion is treated as the master trajectory and the AM-PGM grating is controlled as the follower axis to maintain time-consistent tracking during continuous scans. The FPGA performs real-time control to dynamically drive the Active Mirror–Plane Grating Monochromator (AM-PGM) grating so that it continuously tracks the EPU66S undulator gap during energy scans. A system-on-chip (SoC) FPGA based backend with an FMC ADC module is employed as the beamline-local deterministic data-acquisition backend. System functionality has been validated through hardware-in-the-loop testing using simulated motion trajectories. This EPICS-integrated architecture provides a scalable, beamline-independent solution prepared for future commissioning of undulator-based on-the-fly scanning systems.

INTRODUCTION

On-the-fly scanning [1] eliminates the repetitive start–stop motion inherent in point-to-point acquisition, improving data acquisition efficiency while reducing radiation dose. This approach is widely adopted in synchrotron spectroscopy experiments requiring fast and continuous measurements.

At undulator beamlines, accurate implementation is challenging because photon flux depends on the coupled nonlinear relationship between insertion-device gap motion and monochromator energy. During long continuous scans, network latency and software-trigger jitter can degrade synchronization accuracy. Therefore, deterministic master–follower coordination between the undulator gap and the grating motion is required for stable on-the-fly scans.

To address these challenges, a hybrid architecture combining Experimental Physics and Industrial Control System (EPICS) [2] and Field-Programmable Gate Array (FPGA) is developed. EPICS handles supervisory control and user operation, while deterministic timing, synchronized triggering, and real-time motion tracking are implemented in FPGA hardware. The system is validated through hardware-in-the-loop testing without synchrotron radiation.

BEAMLINE DESIGN

The 35A Soft X-ray Absorption Spectroscopy beamline at the Taiwan Photon Source (TPS) is a soft X-ray beamline driven by an elliptically polarized undulator, EPU66S (period 66 mm, magnetic length 0.8 m) [3], supporting 100–3000 eV via continuous gap tuning. The beamline optical layout and key components are summarized in Fig. 1, highlighting the locations of the two key on-the-fly scan elements: the EPU66S undulator and the Active Mirror–Plane Grating Monochromator (AM-PGM) grating section downstream along the optical path.

For on-the-fly scans, maintaining high photon throughput requires time-consistent coordination between the EPU66S gap trajectory and the AM-PGM grating trajectory during continuous motion. The AM-PGM grating is actuated by a sine-drive mechanism and driven by a stepper motor. The FPGA generates the grating target accordingly so that the grating follows the undulator gap as a follower axis. In the proposed scheme, the EPU66S gap motion is treated as the master trajectory, and the FPGA backend performs real-time control to drive the AM-PGM grating so that it continuously tracks the EPU66S undulator gap over the full scan range, enabling hardware-synchronized on-the-fly scanning (Fig. 1).

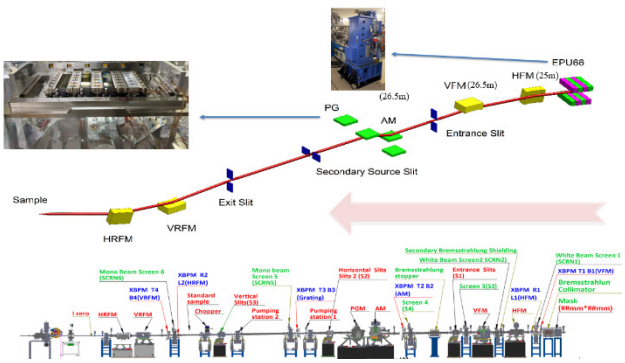

Figure 1: TPS 35A beamline layout highlighting the two key on-the-fly scan elements, the EPU66S undulator and the AM-PGM grating section downstream along the optical path. The undulator gap motion provides the master trajectory, while the grating position is tracked as the follower motion during continuous scans.

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SYSTEM ARCHITECTURE

The control system is organized into three functional layers: an EPICS supervisory layer that provides scan configuration, sequencing, monitoring, and user interaction; an FPGA real-time backend that executes time-critical functions including deterministic data acquisition, trigger generation, and real-time grating tracking; and a beamline instrumentation layer that comprises position feedback components and motion-control hardware.

In the beamline instrumentation layer, both the ID position (EPU66S undulator gap axis) and the grating position (AM-PGM grating axis) are read out from BiSS-C serial absolute encoders. The resulting encoder data provide deterministic and time-consistent position feedback to the FPGA backend for on-the-fly synchronization. A Renishaw absolute optical encoder / readhead is adopted for absolute position measurement [4].

The FPGA/ADC hardware is installed in the beamline local instrumentation rack to minimize analog signal path length and preserve deterministic timing. EPICS communicates with the FPGA backend via Ethernet, ensuring a clear separation between supervisory control and real-time execution. EPICS provides supervisory control, while the FPGA executes time-critical functions including deterministic data acquisition and real-time AM-PGM grating tracking referenced to the EPU66S gap motion.

FPGA HARDWARE IMPLEMENTATION

The FPGA hardware backend is built on a ZedBoard platform based on a Xilinx Zynq-7000 FPGA SoC [5] and is interfaced to an Analog Devices EVAL-AD7134FMCZ ADC mezzanine card [6] via an FMC connector. The FPGA based backend executes deterministic data acquisition, hardware triggering, and real-time tracking functions required for on-the-fly synchronization, while EPICS provides supervisory configuration and monitoring. The hardware setup is shown in Fig. 2.

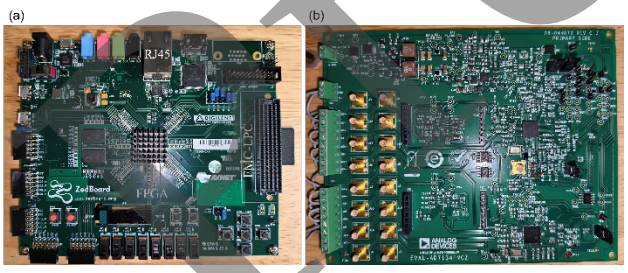

Figure 2: Hardware implementation of the deterministic backend: (a) ZedBoard (Xilinx Zynq-7000 FPGA) (b) Analog Devices (EVAL-AD7134FMCZ).

Deterministic Data Framing

The FPGA data-acquisition logic packages time-aligned measurements into a unified data frame for efficient retrieval by the backend computer. Each frame includes one global time tag, four position channels (encoder/position data), and eight ADC channels (measurement and diagnostic signals). This design enables single-command access to time-synchronized data and simplifies correlation between analog signals and motion states.

Real-time Grating Tracking

In this work, grating tracking is implemented as a fixed master–follower scheme: the EPU66S undulator gap motion is treated as the master trajectory, and the AM-PGM grating is controlled as the follower axis during on-the-fly scans. The FPGA executes deterministic real-time logic to generate the motion command and pulse train required to drive the stepper motor so that the grating continuously follows the master motion over the full scan range.

As illustrated in Fig. 3, the FPGA first translates the measured ID position into a corresponding grating target using the "ID to Grating position translate" block. The "Position Calculate" block then combines the translated target with the measured grating position feedback (GR position) to form the tracking command required for grating motion. The resulting command is routed through a selector (0/1) and delivered to the motor controller, which actuates the grating axis. In the normal on-the-fly operation reported in this paper, the selector is fixed to the tracking path so that the AM-PGM grating always follows the EPU66S gap motion.

EPICS is used only for supervisory configuration, scan sequencing, and monitoring (e.g., loading scan parameters and calibration/mapping data, arming/start–stop control, and status reporting), while all time-critical tracking and synchronization functions are executed in FPGA hardware to minimize latency and timing jitter.

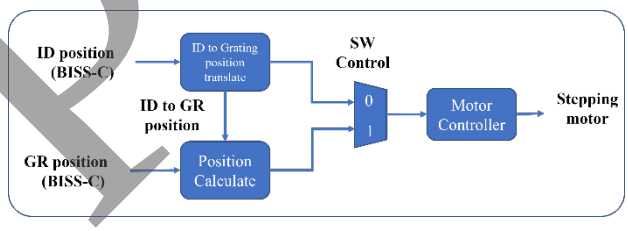

Figure 3: FPGA based grating tracking control logic. The ID position is translated to a grating target ("ID to Grating position translate"), combined with grating position feedback in "Position Calculate", and routed to the motor controller to drive grating motion.

ON-THE-FLY SCAN CONTROL FLOW

Figure 4 shows a typical on-the-fly control flow for an undulator beamline. The scan is initialized by setting the start and end energies (E1–E2). The control system first checks the undulator status and waits until the undulator becomes idle, ensuring the motion subsystem is ready for continuous operation. When the undulator (EPU66S) starts continuous motion from E1 toward E2, detector signals are streamed to the FPGA for continuous data acquisition, while encoder readbacks are simultaneously delivered to the FPGA motion-control block. The FPGA uses the encoder information to generate motor-control commands for the AM-PGM grating axis and maintains synchronized grating tracking, with grating encoder feedback returned to the motion-control loop. During the scan, elapsed time is

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monitored; the scan is terminated when the elapsed time exceeds the predefined (estimated) acquisition duration, ensuring full coverage of the configured scan interval.

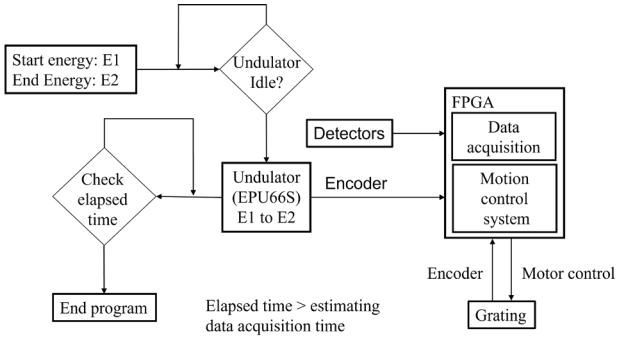

Figure 4: A Typical On-the-fly Control Flow for Undulator Beamline. Continuous undulator motion triggers FPGA data acquisition and synchronized grating motion control, the scan ends when elapsed time exceeds the estimated acquisition time.

EPICS IOC IMPLEMENTATION

Dedicated EPICS Input/Output Controllers (IOCs) were developed to provide supervisory beamline control for on-the-fly scan operation. The IOCs expose scan configuration, execution control, and system status as EPICS process variables (PVs), enabling users to operate the system with standard EPICS tools and ensuring seamless integration into the TPS control environment. The EPICS layer is responsible for scan parameter setup (e.g., energy range and acquisition settings), operation flow management (arming, start/stop sequencing, and fault handling), and continuous status monitoring.

EPICS does not participate in hard real-time loops. After scan initialization and arming, all time-critical functions—including deterministic triggering, synchronized data framing, and real-time grating tracking referenced to the EPU66S gap motion—are executed within the FPGA backend. This partitioning avoids network-induced timing jitter in critical paths while retaining EPICS flexibility for beamline operation and commissioning.

SYSTEM VALIDATION AND STATUS

Because TPS 35A is still under construction, the system has been validated using hardware-in-the-loop testing. Simulated undulator trajectories and corresponding grating mapping profiles were used to verify deterministic triggering and stable acquisition framing, and robustness of EPICS–FPGA supervision (arming, start/stop, status reporting). The tests confirmed stable scan execution suitable for beam-based commissioning once the TPS 35A beamline becomes available.

CONCLUSION

An EPICS–FPGA integrated on-the-fly scan control system has been developed for the TPS 35A undulator beamline. EPICS provides supervisory beamline control, while the FPGA backend executes deterministic data acquisition and real-time AM-PGM grating tracking so that the grating continuously follows the EPU66S gap trajectory over the full scan range during continuous scans. The system has been validated through hardware-in-the-loop testing and is prepared for future beam commissioning.

ACKNOWLEDGMENT

The FPGA based “A Typical On-the-fly Control Flow for an Undulator Beamline” concept was proposed by H.-S. Fung, and the FPGA hardware/firmware backend was developed by C.-Y. Lee. The EPICS IOC modules and the user interface were developed by C.-Y. Lin.

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