PROGRESS OF DEVELOPING THE BUNCH-BY-BUNCH FEEDBACK SYSTEM FOR THE CSNS RCS*

W. Chen, B. Zhang, C. Xie, R. Qiu, Z. Lu R. Yang† and X. Li
Institute of High Energy Physics, Beijing, China
also at Spallation Neutron Source Science Center, Dongguan, China

Abstract

The Rapid Cycling Synchrotron (RCS) of the China Spallation Neutron Source (CSNS) is being upgraded from 170 kW to 500 kW in the CSNS-II. However, significant beam-intensity-dependent transverse instability has already been observed during routine operation. As the beam power increases further, this instability is expected to become much stronger. To effectively suppress the coherent transverse oscillations induced by impedance wakefields and injection errors, a bunch-by-bunch transverse feedback system is Necessary. This paper reports on the development progress, focusing on the custom wideband power amplifier and the effect of output-chain bandwidth on damping performance. PyHEADTAIL simulations are performed to quantify how the low-frequency cutoff affects the damping rate, providing guidance for the design and commissioning of the system.

INTRODUCTION

The China Spallation Neutron Source (CSNS) is a high-intensity proton accelerator facility consisting of a linear accelerator (LINAC) and a Rapid Cycling Synchrotron (RCS) [1]. Currently operating at 170 kW, CSNS is undergoing the CSNS-II upgrade that will raise the beam power to 500 kW by increasing the LINAC injection energy from 80 MeV to 300 MeV and adding supplementary RF systems [2]. As the beam intensity increases, transverse instabilities driven by space charge and coupling impedance become a critical challenge [3,4]. Unlike electron rings, proton synchrotrons lack synchrotron-radiation damping; once excited, instabilities cannot decay naturally and must be suppressed by active means. A bunch-by-bunch transverse feedback system is therefore essential for stable high-power operation, as demonstrated at SNS, J-PARC, ISIS, and the CERN PS.

In a bunch-by-bunch feedback loop, the output chain—consisting of the power amplifier (PA) and the stripline kicker—must deliver a correction pulse that remains uniform over the entire bunch length. This requires the PA to provide both a sufficiently low low-frequency cutoff to minimize pulse droop and a sufficiently high high-frequency cutoff to ensure fast rise and fall times. For the CSNS RCS, where the bunch length reaches 800 ns and the revolution frequency sweeps from 1.02 MHz to 2.44 MHz within a 20 ms acceleration cycle, the existing tune-measurement power amplifier (bandwidth 1 MHz–8.5 MHz) is inadequate for feedback service. A preliminary system design and the key requirements were presented in a previous report [5]. This paper reports on the subsequent development progress, concentrating on two aspects: the custom-developed wideband power amplifier and a simulation study quantifying how the output-chain low-frequency cutoff affects damping performance. Brief updates on the analog front-end and digital signal processing subsystems are also given.

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† yangrenjun@ihep.ac.cn

Table 1: Key System Design Parameters

Parameter	Value
Revolution frequency	1.02 MHz–2.44 MHz
Harmonic number	2
Feedback bandwidth	10 kHz to >10 MHz
Target damping time	0.5 ms
Feedback delay	5-20 turns
BPM signal range	0.1 Vpp–50 Vpp

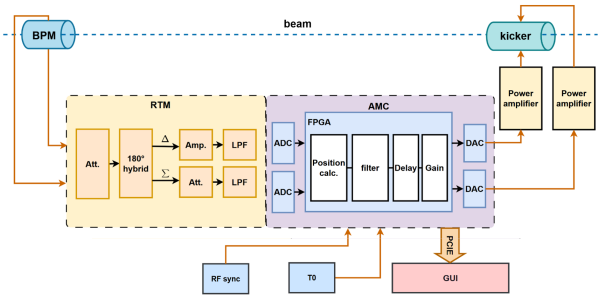

Figure 1: Block diagram of the transverse feedback system.

SYSTEM OVERVIEW

The feedback system comprises a shoebox-type BPM pick-up, analog front-end electronics, a digital processing unit (MTCA.4 standard with SIS8300-KU digitizer: 10 ADC channels at 125 MS / s / 16–bit, Xilinx Kintex Ultrascale FPGA), and an output chain of power amplifier and stripline kicker (Fig. 1). The BPM and kicker are adapted from the existing tune measurement system. Key design parameters are listed in Table 1.

POWER AMPLIFIER

Bandwidth Requirements

In a bunch-by-bunch feedback system, the digital processor computes a single correction value per bunch per turn from the measured bunch centroid position. This correction

Table 2: Power Amplifier Performance Comparison

Parameter	Existing	HPABSC
Frequency range	1 MHz–8.5 MHz	5 kHz–100 MHz
Gain	61 dB	68.5 dB
P_{1dB}	1000 W	1500 W
Gain flatness	–	±2 dB
Spurious	−40 dBc	−75 dBc

is applied as a voltage pulse to the stripline kicker. The feedback loop is designed to damp the rigid dipole mode (mode 0), in which the entire bunch oscillates as a rigid body. For effective correction, all longitudinal slices of the bunch must experience the same transverse kick; otherwise, particles at different longitudinal positions receive different momentum changes. A non-uniform kick has two adverse effects. First, it reduces damping efficiency for the zero-mode, since only a fraction of the bunch is properly corrected. Second, it couples energy into internal head-tail modes, which the feedback loop is not designed to suppress and may even drive.

The output pulse uniformity is therefore a direct requirement on the power amplifier's low-frequency response. The inter-stage coupling and impedance-matching networks of a high-power amplifier introduce an inherent high-pass characteristic, which can be modeled as a first-order RC filter. When a rectangular pulse of duration T_p is applied, the output voltage during the flat-top decays as $V_{\text{out}}(t) = V_0\, e^{-t/\tau}$, where $\tau = RC$ is the circuit time constant. The relative pulse droop is $\text{Drop} = 1 - e^{-T_p/\tau} \approx T_p/\tau$ for $T_p \ll \tau$. Using $f_L = 1/(2\pi\tau)$, the required low-frequency cutoff is

$$f_L > \frac{1}{2\pi} \cdot \frac{\text{Drop}}{T_p}. \tag{1}$$

For the CSNS RCS, with a maximum bunch length of 800 ns and a target droop below 5 %, Eq. (1) gives $f_L \gtrsim 10$ kHz. The high-frequency cutoff must exceed 10 MHz to ensure rise and fall times below 60 ns, preventing overlap between consecutive bunch feedback pulses.

Amplifier Implementation

Two custom power amplifiers (HPABSC1479, HPABSC1480) were jointly developed with a manufacturer to meet the above requirements. Each amplifier adopts a three-stage cascaded architecture with modular power combining at the output stage. The amplifier test bench and the assembled unit are shown in Fig. 2. Table 2 compares the measured performance of the new amplifier against the existing amplifier previously used in the CSNS RCS. The measured gain is 68.5 dB with a flatness of ±2 dB from 5 kHz to 100 MHz, as shown in Fig. 3. The step response with an 800 ns pulse gives a rise time of 28 ns, fall time of 30 ns, and flat-top droop of 4.5 %, all within design margins. The two amplifiers exhibit a gain mismatch of approximately 1.5 dB, which can be compensated in the digital processor upstream of the amplifiers.

Figure 2: Photograph of the amplifier test bench and the assembled power amplifier unit.

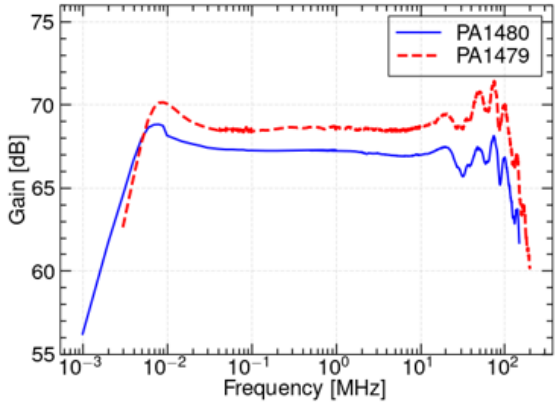

Figure 3: The bandwidth test results of the HPABSC amplifier.

EFFECT OF OUTPUT-CHAIN BANDWIDTH ON DAMPING PERFORMANCE

Simulation Framework

The output chain of the feedback system consists of the power amplifier followed by a stripline kicker. While the amplifier provides a measured bandwidth of 5 kHz–100 MHz, the kicker imposes a high-frequency limitation of approximately 10 MHz, setting the overall upper bound. To evaluate how the low-frequency cutoff f_L of this combined output chain affects damping, a closed-loop simulation was performed using the PyHEADTAIL [6] macro-particle tracking code.

The simulation implements a simplified feedback loop within the PyHEADTAIL one-turn-map framework, considering only the horizontal (x) direction. At each turn, the bunch centroid position is extracted from the particle distribution (ideal BPM), a 90° phase-advanced correction signal is computed (ideal digital processor), and a transverse kick proportional to this signal is applied after passing through the bandpass output-chain model. The simulation incorporates CSNS RCS machine parameters: particle intensity 7.8×10^{12} ppp (corresponding to 170 kW operational beam power), beam energy 1.6 GeV at extraction, nominal betatron

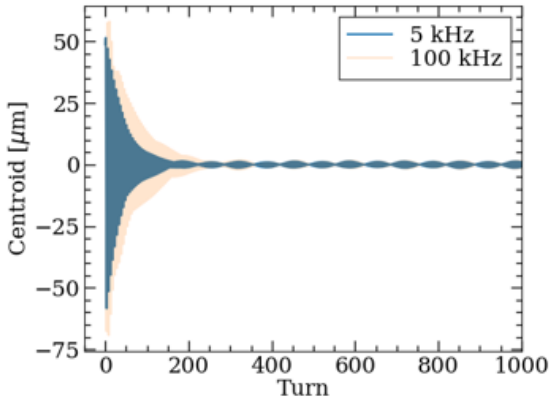

Figure 4: Simulated turn-by-turn oscillation amplitude for $f_L = 5$ kHz (37 turns) and $f_L = 100$ kHz (56 turns). The output chain bandwidth is fixed at 10 MHz; the BPM and digital processing are assumed ideal.

tune $Q_x = 4.86$, and a revolution frequency of 1.02 MHz (fixed at the injection value for this preliminary study). A single bunch of 10 000 macro-particles is initialized with a Kapchinsky–Vladimirsky (KV) transverse distribution, an RMS momentum spread $\sigma_{dp} = 3.25 \times 10^{-3}$, and an RMS bunch length $\sigma_z = 10$ m. The initial betatron oscillation amplitude is set to 50 µm. The output chain (PA + kicker) is modeled as a bandpass system with a fixed upper cutoff at 10 MHz (kicker limit) and a variable first-order high-pass cutoff f_L. The circuit response is implemented as a digital IIR filter applied to the correction waveform before the kick is delivered. The damping time is extracted from an exponential fit to the turn-by-turn oscillation envelope recorded over 2000 turns.

Simulation Results

Two cases were simulated, as shown in Fig. 4. For $f_L = 5$ kHz, the oscillation is damped within 37 turns. When f_L is increased to 100 kHz —with all other parameters unchanged—the damping time extends to 56 turns, representing a degradation of over 50 %. This degradation arises because the higher low-frequency cutoff prevents the output pulse from remaining uniform across the entire bunch, thereby reducing the effectiveness of zero-mode instability suppression. The study confirms that maintaining f_L at the 10 kHz level or below is necessary for effective feedback.

Planned Extensions

The current simulation treats the BPM and digital processor as ideal and models the output chain as a first-order bandpass system. Several extensions are planned to improve the fidelity of the model. A frequency-dependent BPM transfer function based on the shoebox electrode geometry and the measured electrode capacitance will replace the ideal position readout. ADC quantization (16 bit) and front-end thermal noise will be added to the signal path to evaluate their impact on the minimum detectable position offset. The measured power amplifier and kicker bandwidth parameters will be directly incorporated into the output-chain model. These extensions will provide a quantitative prediction of the closed-loop damping rate, supporting parameter optimization before beam commissioning.

STATUS OF OTHER SUBSYSTEMS

The analog front-end (RTM) board design is in progress. The board adopts a three-stage architecture with a 180° hybrid and independent gain conditioning paths for the sum and delta signals, including fast-switch elements to track the 20 dB intra-cycle amplitude variation. Fabrication and bench testing are planned for the next phase.

The digital signal processing firmware is under development on the SIS8300-KU digitizer board. An FIR filter with a lookup-table-driven coefficient update scheme is being implemented to provide closed-orbit suppression and 90° phase advance while tracking the tune evolution during the energy ramp. Laboratory verification using simulated beam signals will follow.

CONCLUSION

The custom wideband power amplifier (HPABSC) has been developed for the CSNS RCS bunch-by-bunch transverse feedback system. The measured bandwidth of 5 kHz–100 MHz with 68.5 dB gain and 4.5 % flat-top droop meets the design specifications. A PyHEADTAIL closed-loop simulation, using measured CSNS RCS beam parameters and a simplified output-chain model, shows that maintaining the low-frequency cutoff at the 10 kHz level is critical: raising f_L from 5 kHz to 100 kHz increases the damping time from 37 to 56 turns. Since the kicker limits the overall bandwidth to approximately 10 MHz, the PA is no longer the bottleneck in the output chain.

The analog front-end RTM design is in progress, with fabrication and bench testing to follow. The FPGA firmware for digital signal processing is under development, with laboratory verification to follow. Integration of the full feedback chain and beam-based closed-loop commissioning at the CSNS RCS are the next major milestones.

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