DIGITAL LOW LEVEL RF SYSTEM FOR ELETTRA 2.0

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Abstract

The new digital electronics of the four Radio Frequency (RF) plants for Elettra 2.0 (E2.0) is fully designed in house, both hardware and firmware. The Digital Low-Level Radio Frequency (DLLRF) works on a non-IQ sampling technique and it is benefiting from the huge internal development of a System On Chip (SoC) Field Programmable Gate Array (FPGA) boards realized for the electron beam position monitor electronics. Each RF plant will have its own machine protection system based on FPGA board to minimize the interlock intervention time. Initial tests of these new electronics have been carried out during last run of Elettra, however the complete commission is carried out using the RF power plant available in the laboratory. This paper presents the design choices and the performed tests that confirm the achievements of the system's specification.

INTRODUCTION

The Elettra 2.0 storage ring will host four identical 500 MHz Radio Frequency (RF) stations, each comprising a 130 kW continuous-wave solid-state amplifier, the 50 Ω WR1800 waveguide section run, a single-cell normal-conducting cavity, and the necessary electronics for RF power control and interlock [1]. The decommissioned Elettra storage ring relied on analog electronics. Today the Low-Level Radio Frequency (LLRF) is being upgraded with up-to-date digital one thanks to this project. This goal can be achieved choosing between a commercial (turn-key) Digital Low-Level Radio Frequency (DLLRF) system and an internal development effort. Even in the last case, it is essential to balance development costs with the reuse or adaptation of commercially available components and boards.

DIGITAL LOW LEVEL RF SYSTEM

A custom DLLRF system—encompassing both hardware and firmware—has been specifically designed for the E2.0 upgrade. The hardware design prioritized modularity, enabling future modifications to be made with minimal cost and implementation impact. The design also adopted a well established, cost effective technology. The DLLRF is divided into two independent subsystems: the digital RF plant interlock and the digital feedback and control system. This architecture boosts redundancy and reliability while allowing each part to be finely tuned to its specific functions. The RF interlock unit acquires all RF plant signals to execute a rapid RF shutdown in response to any potential warning, and forwards the cumulative RF failure status to the general Machine Protection System (MPS) via optical fiber. On top

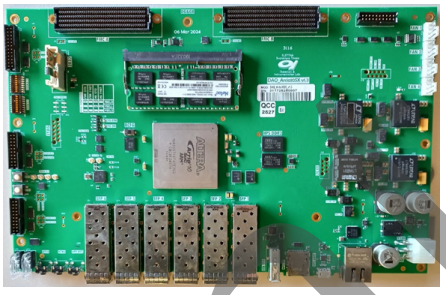

Figure 1: RF Feedback and control mail digital board. Elettra custom development.

of these functions, the RF interlock unit can swiftly shut off the RF for beam dumping, with the operation triggered by an external request. The feedback and control system, in addition to amplitude, phase, and frequency tuning feedback, will carry out the RF power switching on procedure, will follow the proper procedure during externally triggered beam dump, and will record all primary RF signals at the storage ring Turn by Turn (TbT) rate for diagnostics and offline analysis. A pivotal element of this project is the Field Programmable Gate Array (FPGA) based digital board, built around an Altera/Intel Arria 10 and developed in house at Elettra. The board can host two FMC modules, incorporates Double Data Rate (DDR)3 RAM, and offers 10 Gbit/s Ethernet links [2]. It has been further upgraded with a System On Chip (SoC) architecture, as shown in Fig. 1. The board serves as the core of the electron Beam Position Monitor (BPM) diagnostic system; more than one hundred units have been built, and are commissioned and ready for installation in E2.0. Because the entire deployment is well understood and widely distributed, any future issues or bugs can be promptly addressed, and the rapid obsolescence of key components—especially the FPGA and CPU chips—can be managed effectively.

RF INTERLOCK

Handling several kW of RF power requires a reliable and rapid response in the event of any failures. The interlock's electronics feature a robust design based on the Altera Cyclone V GX development board. Additional boards have been designed to condition and monitor more then thirty status signals—water flow rates, temperature, arc detection, amplifier status, and other relevant parameters. Two Analog-to-Digital Converter (ADC) units enable the acquisition of several analog signals, such as cavity vacuum pressure, tuner position and RF drive level. Upon any failure, the digital board actuates a dedicated RF switch to open the RF branch that drives the high power RF amplifier, and simultaneously signals the fault to the MPS via optical fiber. The interlock

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status and ADC data are written to a circular buffer memory that can be downloaded on demand—triggered by an external event—for offline analysis and further verification. Each interlock status is latched to enhance fault identification. Interlock hardware is divided into two units: the digital unit that handles data acquisition and switch control, and the RF unit that houses the switch used to isolate the RF path towards the RF power amplifier.

The implemented RF switch is the SPDT ZX80-DR230 from Mini-Circuits thanks to the fail-safe feature. Its key parameter at 500 MHz, are: open path isolation > 79 dB, close path insertion loss 0.83 dB, return loss > 17 dB. Switch position feedback is provided by a dedicated power detector (Mini Circuits ZX47 40).

The interlock digital unit was successfully commissioned in passive mode during a previous run at Elettra, without RF switch control, while duplicating all monitored signals. When the RF switch control is added, the measured response time from the commutation signal is below 2.5 µs (see Fig. 2).

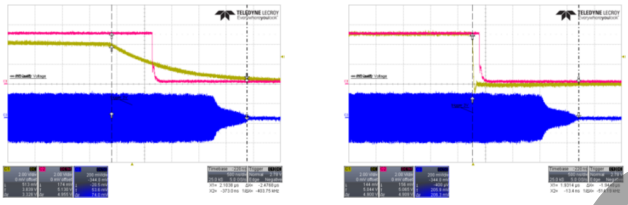

Figure 2: Scope traces: fuchsia: RF switch command; blue: RF output signal. Yellow signal on the left: dry-contact signal switched; on the right: TTL signal switched.

FEEDBACK AND CONTROL

Table 1 lists the cavity field amplitude, phase stability, and frequency tuning specifications for E2.0. The project prioritizes robustness and reliability over extreme performance.

Table 1: E2.0 RF Feedback and Control Main Specification

(a) Feedback Parameters

Parameters	Amplitude	Phase
Control stability	±0.1 %	±0.1°
Accuracy	< 1 %	< 2°
Resolution	< 0.05 %	< 0.05°
Set point range	> 5 dB	> 60°
Dynamic range	> 26 dB	> 10°
Bandwidth	> 20 kHz	> 20 kHz

(b) Frequency Tuning Parameters

Parameters	Value
Dead band	±100 Hz
Hysteresis	±200 Hz
Resolution	≤ 100 Hz
Dynamic range	±200 kHz
Feedback speed	≤ 1 kHz/s

Table 2: FE Early Measurements Results

Parameter	Measured value
Gain conversion (SC21)	−11 dB
Crosstalk	≤−65 dB
SFDR	≤−80 dB
LO leakage	≤−90 dB

Hardware

The hardware architecture is organized into three core units: the FPGA-based processing unit, the Front-End (FE) module (Fig. 4) and the Local Oscillator (LO) and Signal Clock Generator (SCKL) for the reference oscillator and clock distribution for the entire system. The digital board (Fig. 1) has been complemented with four 16 bit, 210 Ms/s LTC2107 ADCs to sample the four Intermediate Frequency (IF) signals, and with two Digital-to-Analog Converter (DAC)s – one to drive the RF output and the other for calibration purposes and as a spare RF output. A custom16 pin GPIO handles connections to the RF Interlock unit, external trigger signals, and the storage ring's TbT signal and counters. I/O communication with the interlock units provides full control over the feedback procedures whenever an RF failure occurs. I/O with external triggers and TbT signals synchronizes the data output stream at the storage ring revolution frequency, 1.16 MHz, with a specific event or turn count.

As illustrated in Fig. 3, the RF signals are first down converted to an 18.5 MHz IF. This approach allows for a more relaxed specification for sampling clock jitter and phase error measurement compared with direct sampling of the 500 MHz RF, without sacrificing performance. Preliminary tests performed on the FE unit show good agreement between the measured results and the specifications of the employed components, particularly with regard to the conversion gain of the individual branches, consistent with the passive nature of the system. The corresponding measured values are summarized in Table 2. At the system level, the measured crosstalk between the active channel and the inactive ones under worst-case conditions, the Spurious-Free Dynamic Range (SFDR), and the LO leakage toward the IF port are within acceptable limits for integration into the signal conditioning chain.

The LO frequency is generated using a Direct Digital Synthesis (DDS) block, with the Analog Devices AD9914 as its core component. Measured integrated noise of the LO signal is below −72 dBc/10 MHz. During the last Elettra run with the beam, the cavity signals were sampled in open loop mode and digitized. Non-IQ sampling technique has been adopted [3]. A resolution of 0.01 % in amplitude and 0.005° in phase has been already achieved at 10 % of the full capability of the first LLRF prototype DAC. The intrinsic Proportional-Integral-Derivative (PID) gain of the system reaches 0 dB at 100 kHz.

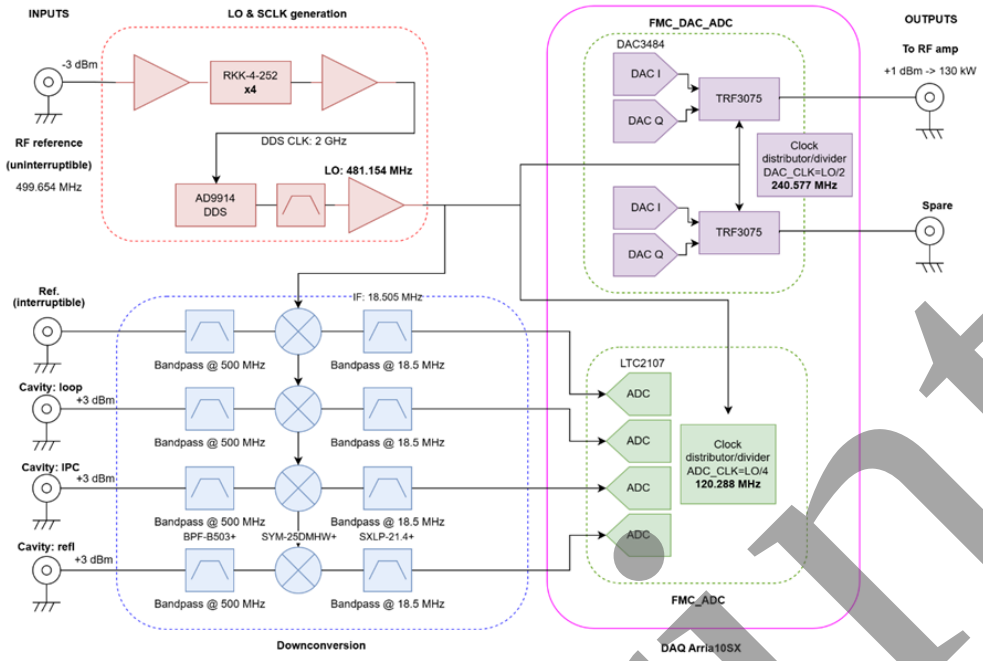

Figure 3: Overview of the three LLRF parts: the Front-End, the Local Oscillator and Signal Clock Generator and the FPGA-based digital platform.

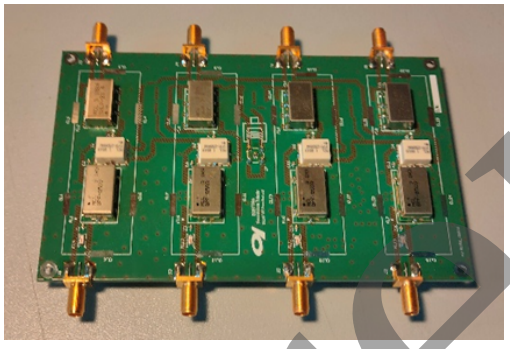

Figure 4: The FE board individual shieldings of each RF path are also foreseen.

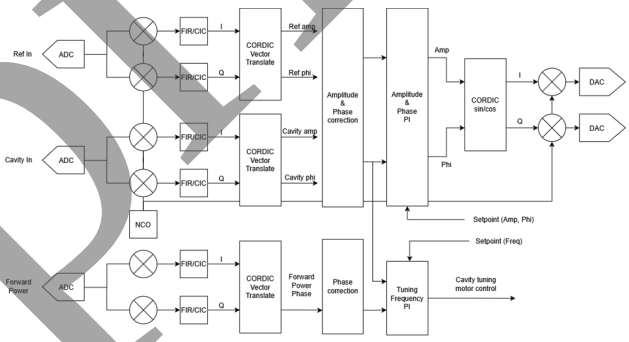

Figure 5: Implemented firmware

Firmware and Initial Result

Two prototype units of the feedback and control system are presently under test in the RF power plant available in the laboratory. The firmware architecture is illustrated in Fig. 5. The amplitude and phase loops can be closed independently for each input signal. A simple user interface allows to set and optimize all the units parameters to commission the system on the real cavity, enabling arbitrary amplitude and phase modulation.

Figure 6 shows the measured performance of the amplitude loop in response to a 50 % duty cycle amplitude modulation at a 1 kHz repetition rate. Phase modulation and frequency offset tests, along with the frequency tuning feedback, are currently underway.

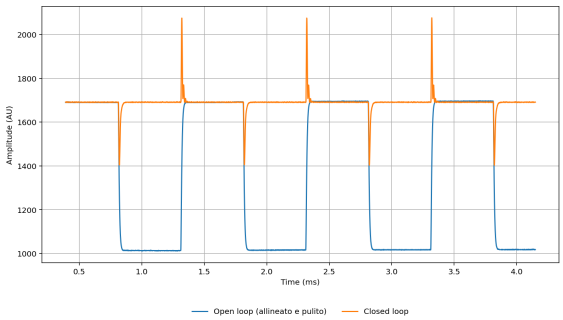

Figure 6: Amplitude-modulated RF signal (blue) and closed-loop control (orange) streaming out at TbT rate. The modulation is a square wave with a depth of 40 % and a frequency of 1 kHz.

CONCLUSIONS

The DLLRF system design has been completed and all the individual boards tested. The RF interlock can cut the RF power delivered to the cavity within 2.5 µs against any RF plant failure. The feedback and control system prototype performance meets the specifications. The DLLRF system can store and stream all the raw data at the storage ring TbT rate becoming a powerful diagnostic tool.

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