

PRELIMINARY DESIGN AND PERFORMANCE VERIFICATION OF A HIGH-POWER, WIDE DYNAMIC RANGE BPM ANALOG FRONT-END FOR THE CSNS-II RCS*

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Abstract

The power upgrade of the China Spallation Neutron Source Phase II (CSNS-II) requires the Rapid Cycling Synchrotron (RCS) BPM system to operate under an extreme 68 dB ultra-wide dynamic range (20 mV to 50 V) and high signal power. The primary design challenges are mitigating thermal drift, suppressing reflections from impedance mismatch, and enhancing low-energy SNR. This paper presents the preliminary design and performance validation of an analog front-end board, adapting successful solutions from facilities like J-PARC MR. The design integrates thin-film resistor attenuators with an impedance tuning network for improved stability and reflection control. Crucially, a hybrid fast/slow switching attenuation strategy is applied: millisecond-level slow switching handles macroscopic changes, while innovative nanosecond-level fast switching enables dynamic gain conditioning during acceleration, significantly boosting the system's SNR. Performance verification results (including attenuation and S21 characteristics) confirm the feasibility and core metrics of the circuit under high-power conditions, providing essential technical guidance for the final implementation at the CSNS-II RCS.

INTRODUCTION

Background and Engineering Challenges

The CSNS-II RCS upgrade raises beam power to 500 kW, increasing BPM electrode signals from about 10-20 V to 50 Vpp and requiring a front-end dynamic range above 68 dB. This creates three main analog front-end challenges: high-voltage/high-power input handling, thermal drift with cable-impedance reflections, and low SNR at injection.

The design follows the J-PARC MR upgrade approach [1, 2], using high-power thin-film attenuators, impedance tuning, and hybrid fast/slow switching.

This paper reports the CSNS-II RCS RTM analog front-end design, domestic thin-film attenuator characterization, and single-channel prototype results, extending previous BPM electronics work [3].

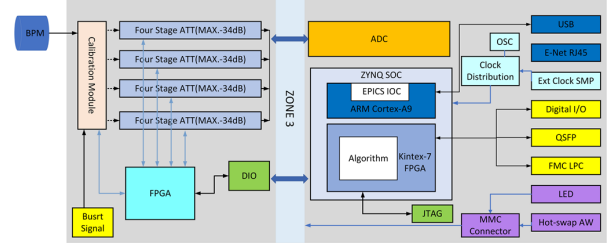


Figure 1: New BPM Electronics Architecture (MTCA.4).

SYSTEM ARCHITECTURE

Overall System Layout

As illustrated in Fig. 1, the BPM electronics use a MicroTCA.4 architecture with an RTM analog front-end and AMC digital back-end. The RTM performs attenuation, impedance matching, calibration, and hybrid switching; the AMC handles sampling, FPGA processing, EPICS control, and communication.

Analog Front-End Signal Chain (RTM)

To cover 20 mV to 50 Vpp, the RTM uses the chain shown in Fig. 2: a 12 dB high-power attenuator with impedance tuning, reed relays for slow switching, ADG5412 analog switches for sub-microsecond gain changes, a second attenuator, a 25 MHz low-pass filter, and in-situ calibration.

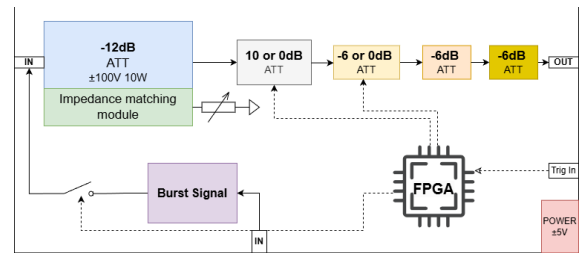


Figure 2: Detailed Block Diagram of RTM Analog Front-End.

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COMPONENT SELECTION AND CHARACTERIZATION

Signal Power Estimation

For 500 kW operation, Fig. 3 shows a maximum electrode signal of 50 V peak-to-peak. With 50 ohm impedance and a 40 ms cycle, average power is about 0.48 W and peak power approaches 50 W.

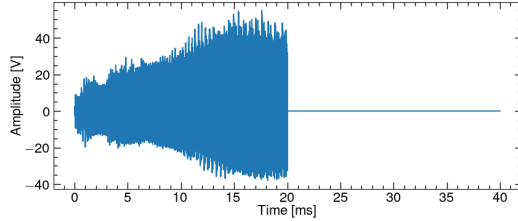


Figure 3: Signal Power Estimation under 500 kW Operation.

First-Stage High-Power Attenuator

The first-stage attenuator is critical. The Hirak RF-20033 (12 dB, 10 W, ± 100 V) was used as a reference, and a domestic metal thin-film attenuator was fabricated with the multilayer structure in Fig. 4. Table 1 summarizes the material comparison used to optimize TCR and thermal behavior.

Table 1: Performance Comparison of Resistor Materials [4]

Material Type	Main Components	Sheet Resistance Range	TCR (ppm/ $^{\circ}$ C)
Ni-Cr Alloy	Ni80Cr20	50-300	± 50
Tantalum Film	TaNx	10-1000	± 100
Gold Film	Au	0.1-10	3000

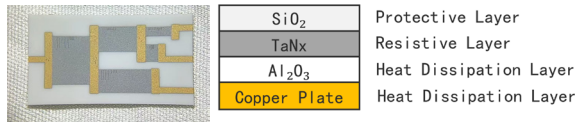


Figure 4: Photograph of the domestic first-stage high-power attenuator and schematic of its multilayer structure.

Test results show that the domestic attenuator achieves comparable power handling, attenuation flatness, and impedance tunability to the Hirak RF-20033.

Second-Stage Attenuator and Switching Devices

For the second stage, a Mini-Circuits BAT-10+ attenuator, OKITA HFS-1C-05W reed relay, and ADG5412 analog switch were selected for hybrid slow/fast switching. Table 2 compares relay candidates and Fig. 5 shows the devices.

Table 2: Comparison of Relay Characteristics

Parameters	HFS-1C-054	PD-1C	MSIP-1A
Contact Form	1 Form C	1 Form C	1 Form C
Contact Rating	3 W	10 W	10 W
Breakdown Voltage	200 V	200V	200 V
Mechanical Life	5×10^7	2×10^7	2×10^7



Figure 5: Physical photographs of candidate reed relays.

PROTOTYPE IMPLEMENTATION AND TEST RESULTS

Prototype Test Board

A single-channel RTM prototype based on the J-PARC MR architecture was fabricated with the Hirak RF-20033 as the first-stage attenuator (Fig. 6). Tests covered attenuation, S21, switching, and domestic attenuator performance.

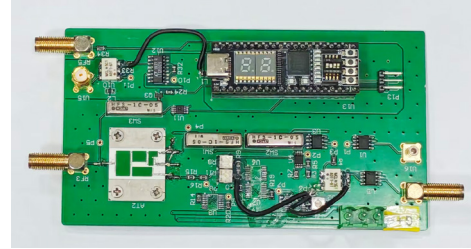


Figure 6: Photograph of the Single-Channel RTM Prototype Test Board.

Attenuation Verification of Each Stage

Calibrated source tests confirmed that the three attenuation stages produced output voltages close to the design values (Table 3).

Table 3: Measured Output Voltage and Calculated Attenuation for Each Attenuator Stage

Parameter	Att. 12dB	Att. 10dB	Att. 6dB	Att. 6dB
Output Voltage (V)	2.42	0.75	0.38	0.19
Calculated Att. (dB)	12.32	10.18	5.90	6.02

S21 Characterization and Hybrid Switching Performance

Network-analyzer measurements in Fig. 7 show flat S21 responses and low insertion loss from 30 kHz to 25 MHz, confirming signal integrity through the attenuation chain. Figure 8 shows millisecond reed-relay switching and a clean ADG5412 sub-microsecond transition with about 120 ns settling.

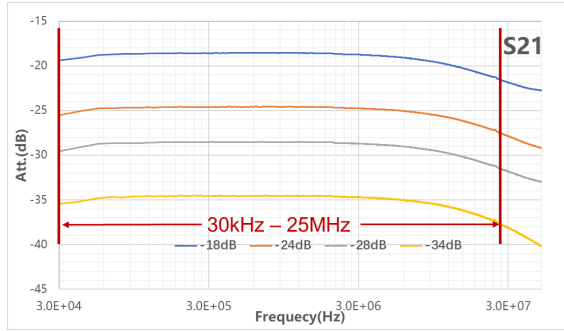


Figure 7: Measured S21 Transmission Characteristics of the Prototype Board with Japanese Hirak RF-20033 Attenuator.

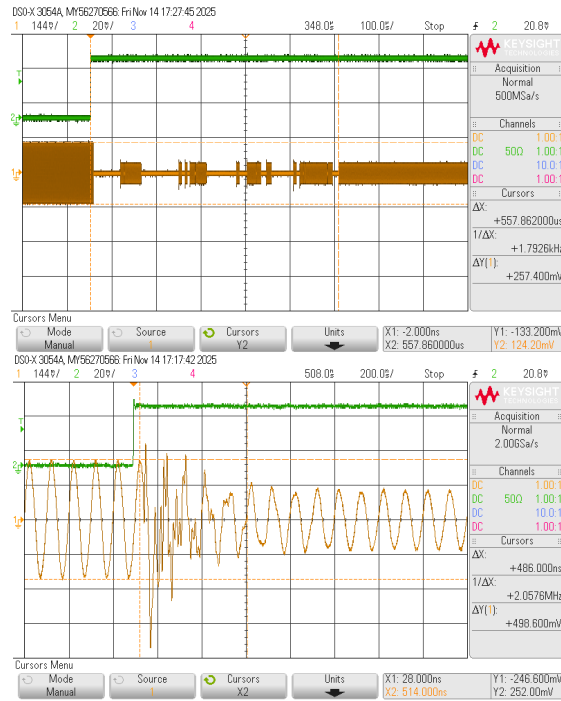


Figure 8: Hybrid Switching Waveforms — Upper: Reed Relay (Slow Switching) Transition; Lower: Analog Switch (Fast Switching) Transition and Settling Time Measurement.

Performance Comparison with Domestic Attenuator

After Hirak RF-20033 baseline tests, a domestic 12 dB metal thin-film attenuator was measured from 1-10 MHz. As shown in Figs. 9 and 10, it maintains good S21 flatness and improved S11 matching after tuning.

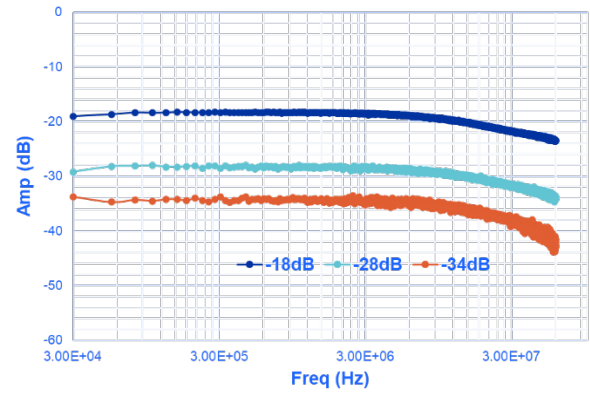


Figure 9: S21 Attenuation Characteristics of the Domestic 12 dB Attenuator.

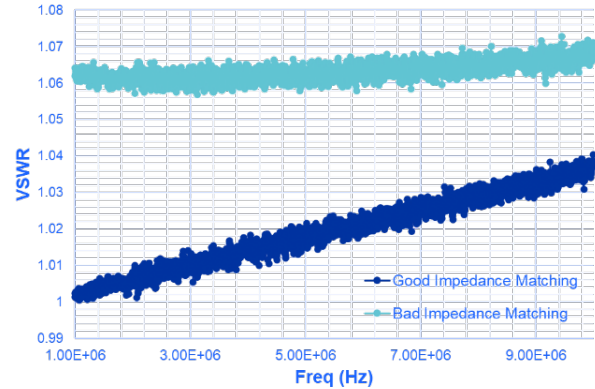


Figure 10: S11 Reflection Coefficient of the Domestic Attenuator (Before and After Impedance Tuning).

The prototype confirms reliable attenuation, impedance matching, hybrid switching, and calibration, supporting multi-channel integration and beam commissioning.

CONCLUSION

A single-channel RTM prototype has verified the multi-stage attenuation and hybrid fast/slow switching scheme under nominal conditions.

The results validate the CSNS-II RCS analog front-end concept and support subsequent multi-channel RTM integration, laboratory characterization, and beam commissioning.

REFERENCES

- [1] K. Satou *et al.*, “The conceptual design study for new BPM signal processing system of J-PARC Main Ring (MR)”, in *Proc. IBIC'23*, Saskatoon, Canada, Sep. 2023, pp. 64-67. doi:10.18429/JACoW-IBIC2023-M0P023
- [2] K. Satou *et al.*, “Status of the new BPM signal processing system for J-PARC MR”, in *Proc. PASJ2022*, Kiryu, Japan, Aug. 2022, paper THP016, pp. 835-839.
- [3] R. Y. Qiu *et al.*, “Optimization and Upgrade of the BPM Electronics System for CSNS-II RCS”, in *Proc. IBIC'25*, Liverpool, UK, Sep. 2025, pp. 829-832. doi:10.18429/JACoW-IBIC2025-WEPM040

- [4] H. Y. Cheng *et al.*, “Developments of Cr-Si and Ni-Cr Single-Layer Thin-Film Resistors and a Bi-Layer Thin-Film Resistor with Adjustable Temperature Coefficient of Resistor,” *Materials Sciences and Applications*, vol. 7, pp. 420-431, 2016.
[doi:10.4236/msa.2016.78037](https://doi.org/10.4236/msa.2016.78037)