

DEVELOPMENT OF AN MTCA.4-BASED DIGITAL LOW-LEVEL RF CONTROL SOLUTION FOR THE TLS LINAC SYSTEM

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Abstract

The Linac of Taiwan Light Source (TLS) has operated for over thirty years, necessitating modernization to ensure sustainability operation. A new digital low-level RF (DLLRF) control system has been developed to replace aging components and address the situation of having only a single backup unit. The MTCA.4 platform was adopted for its scalability and high-performance throughput. The system integrates the DACs module for arbitrary waveform generation with external triggering, and a direct-sampling down-converter with the ADCs module for waveform acquisition and advanced real-time diagnostics. The DLLRF interface has been fully integrated into the EPICS framework for seamless compatibility with existing controls. The new system supports I/Q waveform downloads with online amplitude and phase adjustments, and it provides waveform digitization capabilities for monitoring RF signals associated with the klystron modulator. Dedicated graphical applications have been designed and integrated into the current operator interfaces. The MTCA.4-based DLLRF system has been successfully deployed and validated during routine operations. This paper presents the development, implementation, and operational results of the upgraded control system.

INTRODUCTION

Operational since 1993, the TLS third-generation synchrotron at the NSRRC utilizes an injection chain comprising a 50 MeV Linac, a 1.5 GeV booster, and a storage ring for 360 mA top-up injection. Its control system, originally based on a proprietary VMEbus architecture with Intelligent Local Controllers (ILCs), has migrated to the Linux platform to ensure long-term sustainability. Following successful implementations at the TPS control system [1], the EPICS framework [2] was adopted for TLS modernization. Newly deployed subsystems seamlessly coexist with legacy components within this highly reliable hybrid environment, significantly enhancing operational performance.

The beam quality of a 50 MeV Linac is primarily determined by the stability and flatness of the RF field amplitude and phase. These parameters are highly dependent on the performance of the klystron modulator and beam-loading effects. To circumvent the complex and labor-intensive manual tuning of the pulse-forming network (PFN), an RF feed-forward system [3,4] is implemented for performance enhancement.

TLS pre-injector comprises a 140 kV thermionic gun and a 50 MeV traveling-wave Linac; its schematic layout is illustrated in Fig. 1. The microwave system incorporates a frequency multiplier that converts 499.654 MHz to 2.998

GHz, a 1 kW GaAs solid-state RF amplifier (SSA), and to drive a high-power klystron amplifier. Specifically, the klystron is driven by an 80 MW PFN-based modulator, which is charged by a switching power supply. To regulate the RF field injected into the linac, a vector modulator (VM) output from the DLLRF control unit is positioned upstream of the GaAs amplifier.

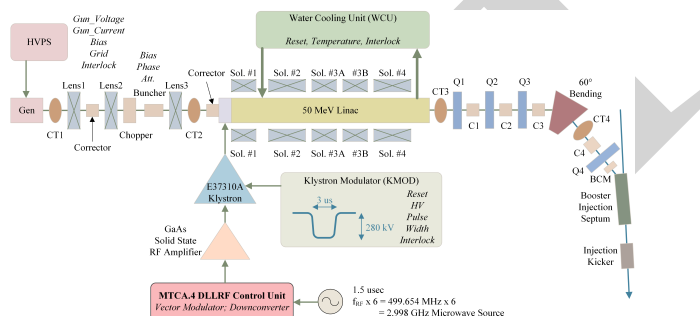


Figure 1: Schematic layout of the 50 MeV TLS linac system, illustrating the pre-injector, klystron, and RF power chain.

Following the migration of the TLS Linac klystron to the E37310A model [5], the DLLRF control system was concurrently upgraded. This transition effectively addressed long-standing challenges regarding the availability of legacy spare parts. The upgrade incorporates mainstream technologies, specifically the MTCA.4 architecture [6], which significantly enhances operational performance, streamlines maintenance procedures, and introduces advanced signal diagnostic capabilities. Over the past decade, the MTCA.4 standard has emerged as a widely adopted framework for DLLRF system modernizations across major accelerator facilities worldwide, where similar platforms have been successfully deployed to achieve unprecedented field stability and advanced diagnostics [7, 8].

Central to this MTCA.4-based platform is the integration of a VM output module and a multi-channel downconverter. This configuration enables real-time monitoring and precise regulation of RF signals across all stages of the Linac system. The newly developed system achieves superior phase and amplitude stability, ensuring highly reliable electron beam acceleration for routine top-up operations.

DIGITAL LOW-LEVEL RF CONTROL SYSTEM FOR TLS LINAC

System Overview

Figure 2 illustrates the functional block diagram of the DLLRF control system for the TLS linac. The architecture is centered on an MTCA.4-compliant control unit, which serves as the computational core for digital feed-forward

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processing. This unit integrates a VM module for signal actuation and a multi-channel downconverter that acts as a high-precision digitizer for monitoring RF signals. To ensure system-wide synchronization, a frequency synthesizer assembly generates and distributes the required clock and local oscillator (LO) signals. The RF power chain subsequently comprises a solid-state amplifier (SSA) and a high-power klystron, the latter of which is driven by a dedicated pulse modulator system.

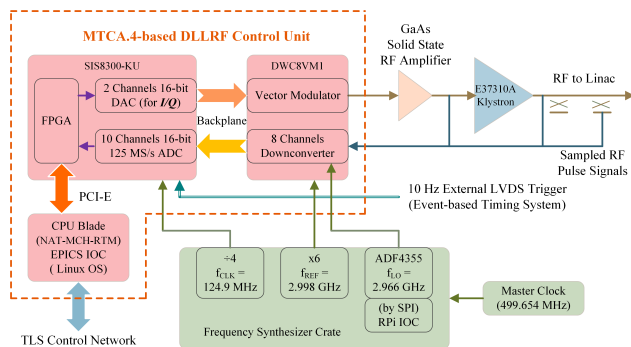


Figure 2: Block diagram of the MTCA.4-based DLLRF system for the TLS linac, featuring a feed-forward control architecture.

Arbitrary waveform data, represented by In-phase (I) and Quadrature (Q) components, are streamed to dual-channel DACs and up-converted via a VM to drive the downstream pre-amplification stage. This technique enables independent RF amplitude and phase regulation, ensuring high drive-signal fidelity and suppressed sideband interference prior to the high-power amplification chain.

The downconverter module translates the high-frequency RF signals from the Linac cavity and klystron output into intermediate frequencies (IF) for digitization. Subsequently, the FPGA-based controller within the MTCA.4 chassis executes high-speed feedback algorithms to modulate the vector modulator, thereby suppressing phase noise and amplitude fluctuations induced by beam-loading or thermal drifts.

Frequency Synthesizer

A frequency synthesizer crate has been developed to generate the multiple synchronized operating frequencies required by the DLLRF system. To clarify the timing infrastructure, a detailed internal schematic of the crate is introduced in Fig. 3. Since overall system stability is critically dependent on frequency synchronization, the crate utilizes the accelerator's master clock (499.654 MHz) delivered from the booster RF system as its primary reference source, which inherently carries an integrated RMS jitter of approximately 300 fs. Within the crate, the internal circuitry employs a sextuple frequency multiplier ($\times 6$) to generate the 2.998 GHz RF reference frequency, while a divide-by-four ($\div 4$) prescaler produces the 124.914 MHz sampling clocks for ADC and DAC operations.

Additionally, an ADF4355 microwave wideband synthesizer [9] with an integrated phase-locked loop (PLL) is utilized to precisely generate the 2.967 GHz LO frequency.

controlled via a Raspberry Pi through an SPI interface [10]. To ensure optimal signal quality, the crate incorporates low-pass filters (LPF) and linear amplifiers, achieving a stable 13 dBm output power. Notably, the final output stages for both the synchronized RF reference and the sampling clocks maintain an ultra-low integrated RMS jitter of less than 300 fs, evaluated within a standard integration bandwidth of 10 Hz to 10 MHz. This experimental result demonstrates that the internal RF amplification and distribution circuitry successfully preserves the reference signal integrity without contributing significant additive noise. This precision timing infrastructure is essential for minimizing phase noise, thereby ensuring the long-term stability of the RF field and the high-resolution performance of the electron beam.

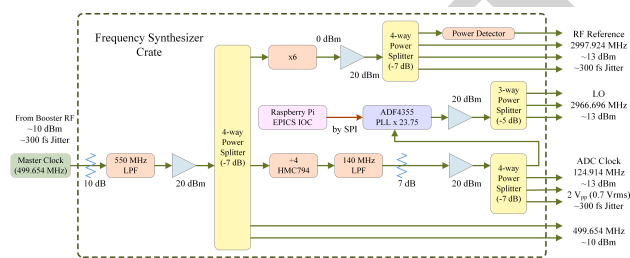


Figure 3: Detailed schematic and power distribution diagram of the frequency synthesizer crate, showcasing the multiplication, division, and PLL synthesis chains.

Control Hardware

The control hardware utilizes a high-performance MTCA.4 AMC card (SIS8300-KU) [11] featuring a Kintex UltraScale FPGA, 10-channel 125 MSPS 16-bit ADCs, and 2-channel 16-bit DACs as the computational core. It is coupled with a Rear Transition Module (DWC8VM1) [12] that integrates an 8-channel downconverter (RF-to-IF) and a single-channel vector modulator. This integrated configuration ensures high linearity, low phase noise, and tight synchronization between the sensing and actuation paths [13] to maintain stringent RF field stability.

Software Architecture and Data Processing

Figure 4 illustrates the software system architecture of the MTCA.4-based DLLRF control system, structured as a multi-layered framework. The system operates within a 64-bit Linux environment running on an Intel Xeon 6-core E-2276ML CPU integrated via a NAT-MCH-RTM module [14] within the MTCA.4 chassis. The framework integrates EPICS v3 as the core middleware, encompassing base modules, an API library driver for software-to-hardware communication, and the FPGA gateway configured by default for downconverter ADC waveform data acquisition.

The Soft IOC (Input/Output Controller) sits at the heart of the stack, managing device support, record processing, and the runtime database. For communication, the system employs Channel Access (CA) protocols to monitor and control Process Variables (PVs), complemented by a Python3-based environment for sophisticated data analysis and automated operations. This layered architecture ensures modularity.

allowing high-level application updates without compromising the stability of the underlying real-time IOC and control loops. Finally, all IOCs and archiver database servers are interconnected via the control network, facilitating seamless console operations and the deployment of high-level applications. This architecture ensures seamless integration and robust interoperability between the DLLRF system and existed control infrastructure, optimizing diagnostic capabilities and monitoring functions.

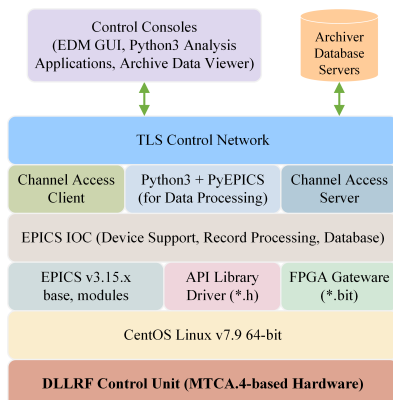


Figure 4: Software system architecture of the MTCA.4-based DLLRF control system.

Operation Interface and Diagnostic Waveforms

To facilitate rapid commissioning and efficient operation of the upgraded DLLRF system, a graphical operator interface has been developed, as shown in Fig. 5. The interface integrates comprehensive control functions for amplitude, phase, and amplitude-delta adjustments used in pulse shaping. Based on the operator-defined parameters, the I/Q waveform data are automatically generated, verified, and synchronously registered at the dual DACs. Once provisioned, these buffered waveforms are played out upon the arrival of an external trigger synchronized with the injection process.

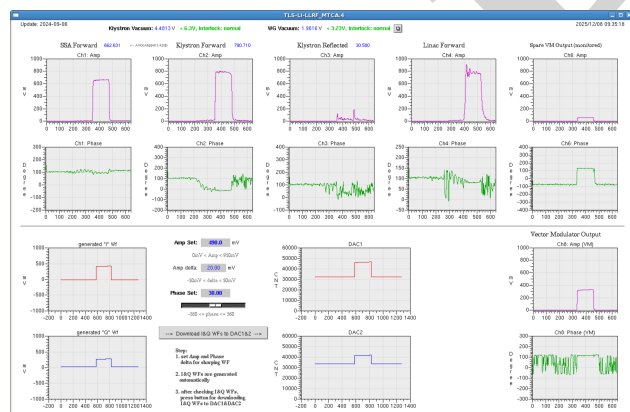


Figure 5: Graphical operation interface of DLLRF control and demodulated waveforms for system diagnostics.

The I and Q components are extracted in real-time from the digitized signals provided by the downconverter ADCs, with the resulting amplitude and phase waveforms visualized on this graphical interface for real-time Linac signal monitoring. Furthermore, key characteristic parameters are

derived from these waveform data to facilitate performance tracking and subsequent stability analysis.

To evaluate this long-term performance, the VM output from the MTCA.4-based DLLRF system was directly routed back to the eighth channel of the downconverter ADC for continuous monitoring. The acquired I and Q components were extracted and demodulated in real-time to compute the amplitude and phase waveforms during each top-up injection. For stability tracking, a characteristic flat-top region corresponding to the electron beam transit was selected; the averaged value within this specific time window was calculated and archived into the database. A dedicated analysis application was developed to retrieve these archived characteristic datasets over extended periods and compute the standard deviation (STD) and root-mean-square (RMS) values to quantify system fluctuations.

Figure 6 presents the statistical distribution of the archived datasets collected over a continuous two-day routine top-up operation period. The experimental results demonstrate that both the amplitude variation (STD/RMS) and the phase variation (STD) remain strictly below the 0.1% threshold. These critical figures of merit successfully quantify the superior stability claimed for this architecture, demonstrating excellent field regulation. Owing to the significantly reduced fluctuations in the MTCA.4-based DLLRF system output, the overall operational stability and reliability have been substantially enhanced, enabling over a year of continuous operation with zero downtime.

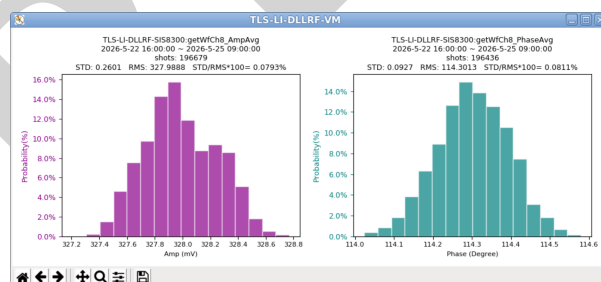


Figure 6: Histograms of demodulated VM output amplitude (left) and phase (right) over a continuous two-day routine operation period for long-term stability analysis.

CONCLUSION

The MTCA.4-based DLLRF control system has been successfully deployed at the TLS Linac, marking a critical milestone in the facility's modernization. Since integration, the system has demonstrated exceptional reliability, achieving over a year of stable, continuous operation with zero downtime. By effectively addressing legacy hardware limitations and ensuring seamless EPICS integration, the new architecture has proven its robustness in a demand Linac environment. Future R&D efforts will focus on advanced FPGA-based control algorithms to further enhance real-time deterministic processing. This successful implementation establishes a sustainable foundation for operational excellence, supporting the long-term evolution of the DLLRF upgrade strategy for the TPS Linac.

REFERENCES

- [1] C. Y. Liao *et al.*, “Commissioning of the TPS Control System”, in *Proc. ICALEPCS'15*, Melbourne, Australia, Oct. 2015, pp. 1173–1176.
[doi:10.18429/JACoW-ICALEPCS2015-FRB3001](https://doi.org/10.18429/JACoW-ICALEPCS2015-FRB3001)
- [2] EPICS, <https://epics-controls.org>
- [3] K. H. Hu *et al.*, “RF Feed-Forward Control Experiments for the 50 MeV Linear Accelerator at TLS”, in *Proc. PAC'07*, Albuquerque, NM, USA, Jun. 2007, paper FRPMN083, pp. 4258–4260.
- [4] C. Y. Wu *et al.*, “An Updated LLRF Control System for the TLS Linac”, in *Proc. NAPAC'16*, Chicago, IL, USA, Oct. 2016, pp. 308–310.
[doi:10.18429/JACoW-NAPAC2016-TUPOA12](https://doi.org/10.18429/JACoW-NAPAC2016-TUPOA12)
- [5] W. Y. Chiang *et al.*, “Current Status of the Upgrade and Operation of the NSRRC TPS LINAC Pulse High-Power RF System”, presented at IPAC'26, Deauville, France, May 2026, paper TUP7647, this conference.
- [6] T. Walter, F. Ludwig, K. Rehlich, and H. Schlarb, “Novel Crate Standard MTCA.4 for Industry and Research”, in *Proc. IPAC'13*, Shanghai, China, May 2013, paper THPWA003, pp. 3633–3635.
- [7] C. Schmidt *et al.*, “Performance of the MTCA.4 Based LLRF System at FLASH”, in *Proc. IPAC'14*, Dresden, Germany, Jun. 2014, pp. 2433–2435.
[doi:10.18429/JACoW-IPAC2014-WEPME067](https://doi.org/10.18429/JACoW-IPAC2014-WEPME067)
- [8] P. Echevarria *et al.*, “LLRF control upgrade at BESSY-II with mTCA.4 platforms”, in *Proc. IPAC'23*, Venice, Italy, May 2023, pp. 4529–4531.
[doi:10.18429/JACoW-IPAC2023-THPL045](https://doi.org/10.18429/JACoW-IPAC2023-THPL045)
- [9] ADF4355, <https://www.analog.com/en/products/adf4355.html>
- [10] Y. S. Cheng, K. T. Hsu, K. H. Hu, D. Lee, and C. Y. Liao, “Application of Soc Based Applications in the TPS Control System”, in *Proc. ICALEPCS'17*, Barcelona, Spain, Oct. 2017, pp. 1569–1572.
[doi:10.18429/JACoW-ICALEPCS2017-THPHA079](https://doi.org/10.18429/JACoW-ICALEPCS2017-THPHA079)
- [11] SIS8300-KU, <https://www.struck.de/sis8300-ku.html>
- [12] DWC8VM1, <https://www.struck.de/dwc8vm1.html>
- [13] C. Xie *et al.*, “Digital low-level RF system for the infrared free-electron laser facility”, *Nucl. Instrum. Methods Phys. Res., Sect. A*, vol. 1040, p. 167071, Oct. 2022.
[doi:10.1016/j.nima.2022.167071](https://doi.org/10.1016/j.nima.2022.167071)
- [14] NAT-MCH-RTM, <https://nateurope.com/product/nat-mch-rtm/>