SOFTWARE DEVELOPMENT OF BEAM DIAGNOSTICS READOUT SYSTEM BASED ON A MULTI-CHANNEL HIGH-SPEED DIGITIZER*

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Abstract

In the upgraded accelerator of the China Spallation Neutron Source Phase II project, several multi-channel beam diagnostic detectors are installed, including a Ionization Profile Monitor for measuring the injection beam profile and a Multi-Wire Profile Monitor for measuring the target beam profile. In the China Spallation Neutron Source, similar multi-channel detectors typically utilize multiple PXIe acquisition cards to construct a PXIe-based signal acquisition system, which suffers from high cost and limited flexibility. This paper presents an alternative signal readout solution using a multi-channel high-speed digitizer to replace the PXIe system. The digitizer incorporates built-in front-end amplification functionality, eliminating the need for separate analog electronics for signal amplification. With a maximum sampling rate of 125 MS/s, it fully meets the sampling requirements for the beam pulse width in the CSNS-II Rapid Cycling Synchrotron, which ranges from 500 ns to 80 ns. Moreover, the multi-channel signal acquisition system implemented with this digitizer offers high integration and reduced cost compared to the PXIe system, making it an ideal choice for beam diagnostics systems.

INTRODUCTION

In the upgraded accelerator complex of the China Spallation Neutron Source Phase II project, the beam diagnostics system employs various multi-channel detectors, such as the Ionization Profile Monitor and the Multi-Wire Profile Monitor. Traditionally at CSNS, signal acquisition for such detectors relies on systems built with multiple PXIe cards. While functional, this approach presents challenges in terms of high cost and system integration complexity. This paper presents the development of a new readout solution centered on a CAEN DT2745B multi-channel high-speed digitizer. The digitizer integrates front-end amplification, eliminating the need for separate analog electronics. Its maximum sampling rate of 125 MS/s is sufficient for the beam pulse widths (80 ns to 500 ns) in the CSNS-II Rapid Cycling Synchrotron. The associated data acquisition and control software, developed in C on the Linux platform and integrated with the Experimental Physics and Industrial Control System, offers a more open, stable, and cost-effective alternative to the previous LabVIEW and PXIe-based system[1].

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HARDWARE ARCHITECTURE

PXIe-Based Acquisition System

The conventional signal acquisition system for multi-channel beam diagnostics detectors at CSNS is built upon a PXIe platform. This architecture typically consists of a PXIe chassis housing a system controller and multiple high-speed multifunction data acquisition cards. Each card provides a limited number of analog input channels . To achieve the required channel count for detectors like the Multi-Wire Profile Monitor, multiple such cards are installed within the same chassis[2]. Separate rack-mounted or custom-designed front-end analog electronics are required for signal conditioning and amplification before feeding signals to the DAQ cards. The system offers high performance and precise synchronization between channels on the same card via the PXIe backplane. However, it results in a system composed of multiple discrete components: chassis, multiple DAQ cards, and external analog electronics, leading to increased system footprint, cabling complexity, and overall cost.PXIe hardware architecture diagram is shown in Fig. 1.

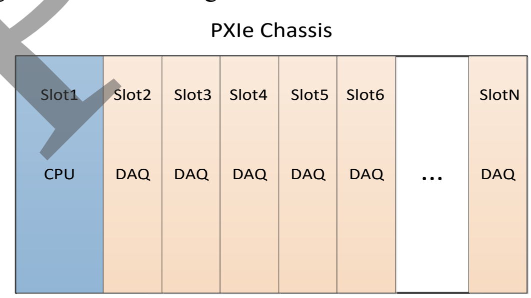

Figure 1: PXIe hardware architecture diagram.

Multi-Channel Digitizer System

The core hardware of the new proposed system is the CAEN DT2745B digitizer. Its key specifications include 64 analog input channels, a 16-bit ADC, a maximum sampling rate of 125 MS/s, and integrated programmable-gain front-end amplifiers (gain range: 0 to 40 dB, adjustable in 0.5 dB steps per 16-channel group). The device features both USB and Gigabit Ethernet interfaces for control and data transfer, and runs a Debian-based embedded operating system on its internal ZYNQ UltraScale+ SoC, allowing for standalone or networked operation. A single DT2745B unit integrates the functions of multiple PXIe cards into one compact device[3][4]. The multi-channel digitizer system diagram is shown in the Fig. 2.

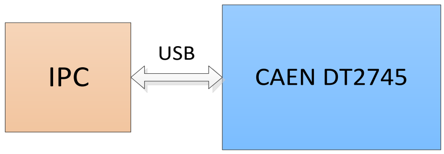

Figure 2: Multi-channel digitizer system diagram.

SOFTWARE ARCHITECTURE

The software architecture is designed for high performance, reliability, and seamless integration with the EPICS-based control system at CSNS. It consists of three main layers:

Driver & Library Layer

This foundational layer includes the CAEN USB driver, communication libraries (CAENComm, CAENVMELib), and the core CAEN_FELib (Firmware Library). The CAEN_FELib provides the essential C API for device control and data streaming.

Data Acquisition Application Layer

A custom multi-threaded C application is developed on top of CAEN_FELib. Its primary role is to configure the digitizer parameters (sampling rate, record length, trigger source, gain, etc.), manage a continuous data acquisition loop, and process the incoming waveform data. The application employs producer-consumer threading to separate the data reading/processing logic from the user interface/command handling, achieving pseudo-asynchronous data readout[5].

EPICS Integration Layer

To publish acquired data and allow remote control, the system integrates with EPICS. A standard EPICS Input/Output Controller is created using the makeBaseApp tool. Within the data acquisition application, the EPICS Channel Access library is used to push processed waveform data to waveform Process Variables hosted by the IOC. This enables any EPICS client to monitor the real-time beam signals.The software architecture is shown in the Fig. 3.

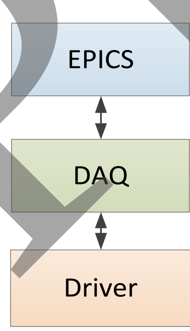

Figure 3: Software architecture.

SOFTWARE COMPONENTS AND FUNCTIONALITIES

To enable multi-channel signal acquisition for multiple IPM, a specialized DAQ software suite has been implemented. Configured with a sampling rate of 125 MSPS, a record length of 600 μs, and 64 acquisition channels, the software components and functionalities is shown in the Fig. 4.

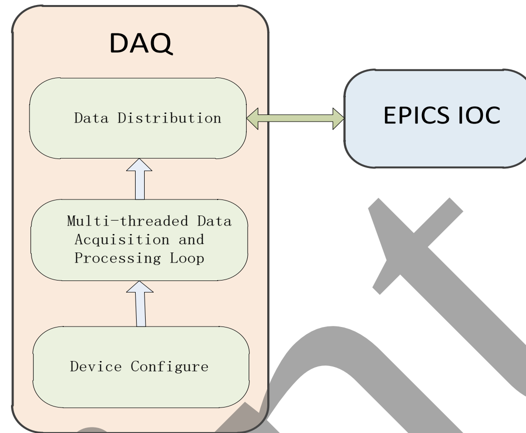

Figure 4: Software components and functionalities.

Device Configuration

The software initializes a connection to the digitizer using a connection string. Key device parameters are configured programmatically through API function: acquisition Parameters, Record length,pre-trigger samples, and decimation factor.

Trigger Settings:the source can be set to external trigger, software trigger, or internal test pulse. The trigger level can be set NIM or TTL.

Channel Settings:Enabling or disabling channels, setting DC offset, and critically, configuring the front-end amplifier gain.

Multi-threaded Data Acquisition Loop

The core acquisition runs in a dedicated thread. It first configures the data readout format using CAEN_FELib_SetReadDataFormat and then enters a loop calling CAEN_FELib_ReadData. This function blocks until a trigger event occurs or a timeout is reached, then returns the event's timestamp, trigger ID, and the raw ADC waveform data for all enabled channels. For each event, the software performs the following processing: ADC to Voltage Conversion: It reads the channel-specific conversion coefficient and applies it to the raw ADC data, translating counts into meaningful voltage values.

Data Save: Processed waveform data can be saved to disk. The software supports saving all events to a single file with timestamps or saving each trigger event to an individual file for easier analysis. The save function is controlled by compile-time macros for flexibility.

Data Distribution

After converting ADC data to voltage, the application uses the EPICS CA library to write the voltage array for each channel to its corresponding waveform PV in the IOC. The PV naming follows a pattern like chXX::waveform. The IOC is configured using a template and substitution file to instantiate 64 waveform records, one for each channel. This design provides a standardized interface for the control system to access the high-speed acquisition data[6].

SOFTWARE TEST

The complete software system underwent extensive testing in the laboratory.

Driver and Basic Communication: The CAEN_FELib library and associated drivers were successfully installed and tested on an Ubuntu industrial PC.

External and Internal Trigger Modes: The software was validated in both external trigger mode and internal test pulse mode. The system correctly acquired data synchronized to the external trigger and generated data.

Data Acquisition and Processing: The custom multi-threaded application was verified to continuously acquire data, convert ADC values to voltages using per-channel coefficients, and print real-time statistics..

EPICS Data Publishing: The integration was tested by running the EPICS IOC and the acquisition application simultaneously. The voltage waveform data published by the application was successfully monitored and retrieved in real-time using standard EPICS tools like caget and Control System Studio graphical operator interfaces.

Embedded Operation:The application was cross-compiled and run successfully on the digitizer's own embedded Debian system, demonstrating the potential for a highly integrated, stand-alone acquisition node.

The signal acquisition system built in the laboratory is shown in Fig. 5.

Figure 5: The signal acquisition system.

The pulse signal and trigger signal output by the signal generator are connected to CH00, CH01, and Trig IN of the digitizer. After running the program, the corresponding waveform PV values are shown in Fig. 6.

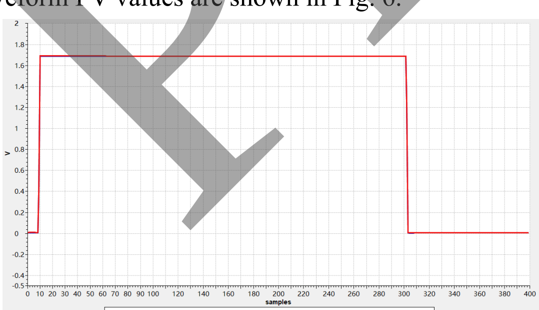

Figure 6: Acquired waveform signal.

A response time test was also conducted. For a trigger frequency of 25 Hz, the response time over a period is shown in Fig. 7. The figure indicates that the response time is consistently around 40 ms.

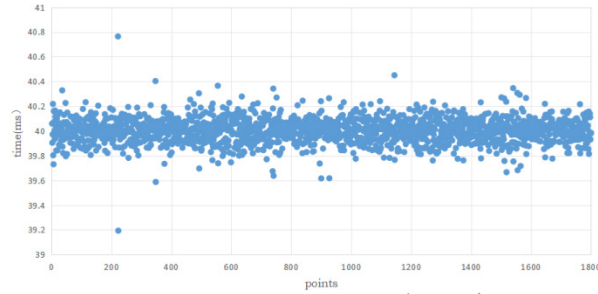

Figure 7: The response time.

CONCLUSION

A new beam diagnostics readout system based on the CAEN DT2745B high-speed digitizer has been developed. The hardware offers high integration (64 channels with built-in gain control) at a reduced cost compared to multi-card PXIe systems. The accompanying software, developed natively in C on the Linux platform, provides robust and efficient data acquisition, processing, and storage. Its deep integration with EPICS, through a standard IOC and the Channel Access library, ensures seamless incorporation into the larger accelerator control system, enabling real-time monitoring and data sharing. This system resolves the stability and openness limitations of the prior LabVIEW/Windows-based solution and has been validated as a reliable and effective platform for multi-channel beam diagnostics signal acquisition at CSNS-II.

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