

The development of new digital BPM signal processor for SSRF*

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Abstract

As part of the intelligent upgrade of the Shanghai Synchrotron Radiation Facility (SSRF), a new digital BPM processor with timestamp-synchronized data has been developed. The processor comprises a digital signal processing motherboard and an RF signal conditioning and sampling daughterboard, and is integrated with a White Rabbit timing board. The motherboard utilizes an MPSoC FPGA as the system controller and signal processing unit. An FMC slot is designed to interface with the White Rabbit timing board, and a high-speed data connector is implemented for the daughterboard, which generates a pilot-tone signal for drift compensation. The resolution of the close orbit data achieves 5 nm. The processor is currently in mass production for the SSRF upgrade.

INTRODUCTION

As part of the intelligent upgrade of SSRF, the BPM system is required to provide high-resolution orbit data with precise timing information for beam commissioning, orbit analysis and future data-driven operation. The main resolution requirements of the new digital BPM signal processor are listed in Table 1.

Table 1: Resolution Requirements of the Processor

Data rate	Resolution (RMS)
Turn-by-turn (694 kHz)	$\cong 1 \mu\text{m}$
Fast acquisition (10 kHz)	$\cong 200 \text{ nm}$
Closed orbit (10 Hz)	$\cong 50 \text{ nm}$

Previous work on digital BPM processors and related front-end modules has provided the technical basis for this development, especially in BPM electronics design and system integration [1-3]. However, the SSRF intelligent upgrade requires full-ring synchronized acquisition, precise timestamping and improved long-term stability. Therefore, a new processor architecture with White Rabbit timing capability is required.

The existing BPM electronics were not originally developed with a unified high-precision timestamp interface, making it difficult to strictly align TBT, FA and SA data from different BPM stations. In addition, limited hardware resources and interface openness restrict further function extension for SSRF-specific applications.

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To meet these requirements, a new digital BPM signal processor has been developed for SSRF. The processor digitizes the conditioned RF signal by band-pass sampling, and combines pilot-tone based drift compensation with White Rabbit timing capability.

ELECTRONICS DESIGN

The new digital BPM signal processor adopts a modular electronics architecture, as shown in Fig. 1. The system mainly consists of an RF signal conditioning and sampling daughterboard and a digital signal processing motherboard. The daughterboard is responsible for analog front-end processing of the four BPM electrode signals, analog-to-digital conversion, sampling clock distribution and pilot-tone generation. The motherboard performs sampled data acquisition, real-time digital signal processing, system control, data transmission and White Rabbit timing interface functions.

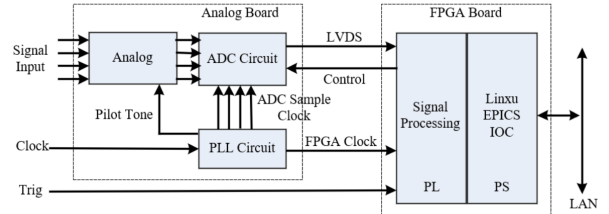


Figure 1: Block diagram of the processor.

RF Daughterboard

The structure of the RF signal conditioning and sampling daughterboard is shown in Fig. 2. It consists of an RF analogue front-end module, a high-speed ADC sampling module, and a PLL module for the generation of sampling clock and pilot-tone.

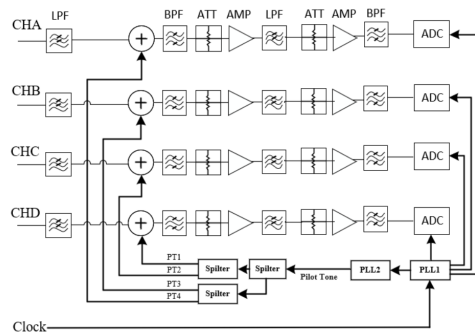


Figure 2: Block diagram of the RF daughterboard.

The RF analogue front-end consists of four chains of ceramic band pass filters (BPF), amplifiers (AMP), low pass filters (LPF) and step attenuators (ATT). It extracts the

BPM signal at 500 MHz with a bandwidth of approximately 24 MHz. The channel isolation is better than 73 dB. The ADC module uses 16-bit ADCs with a maximum sampling rate of 125 MSPS. The PLL module is based on an LMK04832 jitter-cleaner architecture, which generates ADC sampling clocks at 117.284 MHz. The pilot-tone generation module generates a steady calibration signal and sends it to four RF channels for compensation of slow drift. In this design, the pilot-tone frequency is set to $f_{RF} + 2.5f_{ref}$, where f_{RF} is the SSRF storage-ring RF frequency of about 499.654 MHz and f_{ref} is the revolution frequency of about 693.964 kHz. Therefore, the pilot-tone frequency is about 501.4 MHz. The daughterboard is shown in Fig. 3.

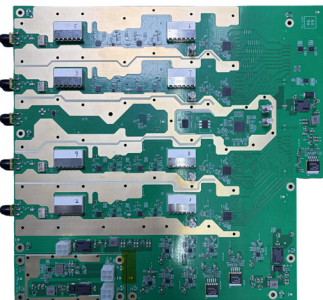


Figure 3: RF daughterboard.

Digital Signal Processing Motherboard

The digital signal processing motherboard is shown in Fig. 4. The motherboard is based on an MPSoC FPGA and serves as the main control and real-time processing platform of the processor.

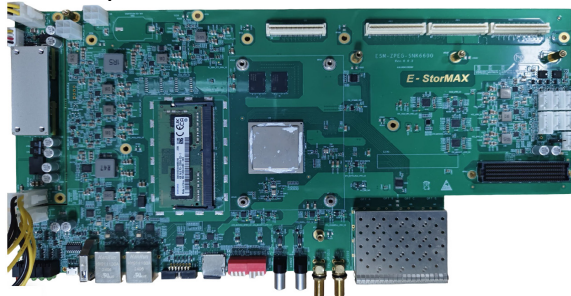


Figure 4: Digital signal processing motherboard.

High-speed data connectors for the RF board and FMC slot for the White Rabbit timing card are designed on the board. Various peripheral interfaces are also featured. The processor is shown in Fig. 5.



Figure 5: BPM signal processor.

The digital signal processing flow is illustrated in Fig. 6. The sampled data of the four channels are first sent to digital down-conversion modules to obtain the amplitude at revolution frequency, which are composed of DDSs, multipliers, CIC filters and decimators, FIR filters and decimators, and CORDIC modules. The beam position is then

calculated by the difference-over-sum algorithm of the four channels.

TBT, FA and SA position data are obtained by multi-stage filter and decimation process. The pilot-tone signal is processed in parallel with the beam signal, and its amplitude information is used for channel drift compensation. The White Rabbit timing information can be bound to BPM data, enabling synchronized data output among different BPM stations.

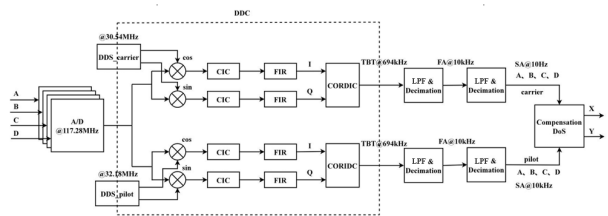


Figure 6: Digital signal processing flow.

The supported data types and maximum acquisition lengths are listed in Table 2.

Table 2: Data Mode

Data type	Mode	Maximum acquisition length
ADC data	Capture	512 M
	Streaming	2048
TBT data	Capture	32 M
	Streaming	1024
FA data (50/10 kHz)	Capture	32 M
	Streaming	1024
SA data	Capture	32 M
	Streaming	

The EPICS IOC and PyDM user interface was developed for system control. The PyDM control panel is in Fig. 7.

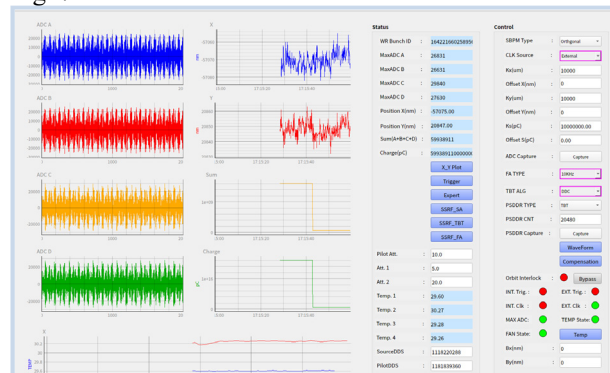


Figure 7: PyDM-based user control panel.

PERFORMANCE TEST

Performance tests were carried with beam at SSRF and with RF source in the laboratory.

Beam Test at SSRF

The beam test was performed at the SSRF storage ring under top-up operation. During the test, the beam current was about 220 mA. The reference clock was derived from

the machine revolution clock, and the White Rabbit timing signal was connected through optical fiber. The BPM pickup signals were combined and divided to generate four equivalent input signals for the processor.

The RMS resolution of TBT, FA, SA data are shown in Fig. 8, Fig. 9, Fig. 10, 400 nm, 70nm and 4.8 nm.

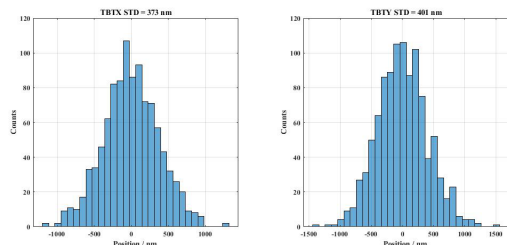


Figure 8: Position resolution for TBT.

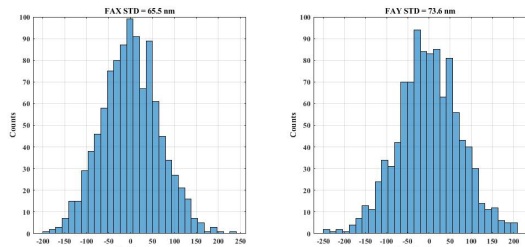


Figure 9: Position resolution for FA.

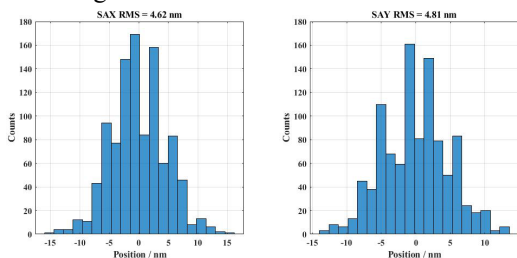


Figure 10: Position resolution for SA.

SA position data of 14 hours is shown in Fig. 11. Blue lines are pre-compensation data, red lines are compensated data. The resolution was 41.5 nm X and 63.4 nmY, after compensation.

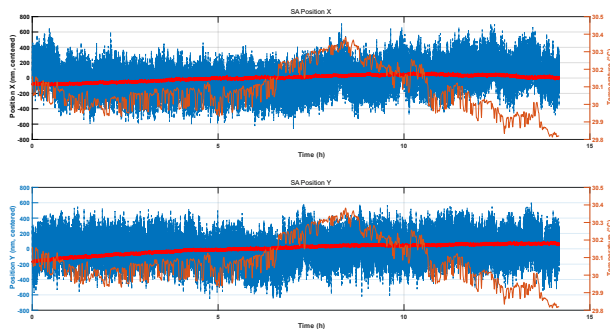


Figure 11: Long-term stability test result.

Laboratory Test

The laboratory test was carried out with a R&S SMW200A signal generator, which generates a 499.67 MHz RF signal and an approximately 694 kHz reference

clock. The RF signal was divided into four equal channels and connected to the four inputs of the processor.

For the beam-current dependence test, the temperature chamber was maintained at 20 °C. The output power of the signal generator was swept from -48 dBm to -4 dBm with a step of 4 dB, corresponding to a single-channel input power from about -54 dBm to -10 dBm after power division. As shown in Fig. 12, the peak-to-peak position variations were 0.67 μm in the X direction and 0.59 μm in the Y direction.

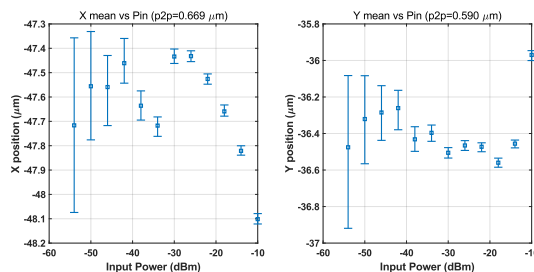


Figure 12: Beam current dependence test result.

The temperature drift test was performed in a temperature chamber. The chamber temperature was increased from 20 °C to 40 °C in steps of 1 °C every 20 minutes. As shown in Fig. 13, the peak-to-peak position drifts were about 0.8 μm in the X direction and 2 μm in the Y direction. The corresponding linear fitting coefficients were about 40 nm/°C and 100 nm/°C, respectively.

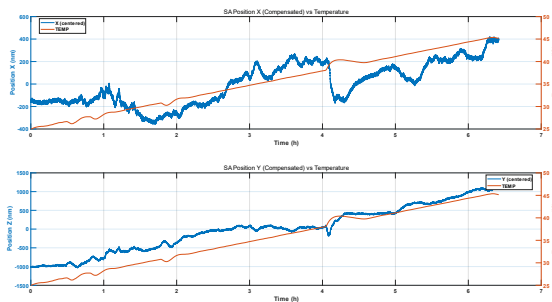


Figure 13: Temperature drift test result.

CONCLUSION

A new digital BPM signal processor has been developed for the SSRF intelligent upgrade project. The measured resolutions are better than the design requirements. The development and integration of the processor have been completed, and is currently in mass production for the SSRF upgrade.

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