SSPA EFFICIENCY IMPROVEMENT STUDIES AT ALBA IN THE FRAMEWORK OF THE RF2.0 PROJECT

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Abstract

ALBA is a 3rd generation synchrotron light source and member of the RF2.0 project, which aims to reduce the carbon footprint of this kind of large research facilities by improving its efficiency, reliability and operational sustainability. In this contribution, we present the work done together with our partner COMMTIA, that has developed an Active Parametrization Digital Control (APDC) for a 5 kW 1.5 GHz SSPA, which enables a real-time efficiency optimization by changing dynamically the drain voltage of the transistors while delivering RF power.

This is done in two different ways: either the SSPA user sets the desired voltage as function of the output power or the Digital Low Level RF (DLLRF) system sets the voltage automatically to the SSPA by means of a digital signal as a function of the input reference value. This maximizes the efficiency at each point of operation, ensuring stable performance under the varying load and thermal environments common on accelerator facilities.

The laboratory measurements indicate substantial improvements in efficiency, that comes with the cost of the SSPA linearity gain reduction. These developments show how flexible solid-state RF systems can fulfil demanding high-performance requirements while lowering the energy consumption and carbon footprint of accelerator infrastructures.

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INTRODUCTION

Synchrotron light sources are large scale scientific infrastructures with significant power consumption, where Radiofrequency systems constitute a significant fraction of the total energy demand. In recent years, increasing emphasis has been placed on improving the energy efficiency and sustainability of these facilities. In this context, the RF2.0 project aims to reduce the carbon footprint of accelerator facilities and one of the strategies is to promote the development of more energy efficient RF sources.

Conventional SSPA typically operate with fixed drain voltages, which results in suboptimal efficiency when the output power deviates from the nominal design point. It is in this context that ALBA together with its partner COMMTIA have developed and tested the APDC that adjust the transistor's drain voltage to maximize the efficiency in the whole power range of the amplifier. This is done even when the amplifier is under operation.

Taking advantage of the SSPA prototype developed by COMMTIA for the ALBA 3rd harmonic system [1], the equipment has been retrofitted and the APDC has been implemented in it. This SSPA is a GaN transistor based high power amplifier. This technology offers higher power density, higher drain efficiency and improved thermal capability due to their wide bandgap characteristics, making them particularly suitable for high-power CW accelerator applications [2, 3].

The SSPA provides up to 5 kW continuous wave (CW) at 1.5 GHz. The SSPA is based on a modular architecture with two identical power amplifier (PA) units, each one is able to deliver up to 2.5 kW. The output of each of this modules is then combined in an hybrid coupler to achieve the required output power.

Each PA integrates multiple transistor-based amplification stages, including LDMOS based driver stages with a final stage of parallel GaN based power transistors. Power combination inside each PA is performed by multi-stage combiners after an individual circulator for each transistor, providing robustness and protection against reflected power due to amplitude or phase mismatches in the combiners. The baseline design achieves an overall AC to RF efficiency of approximately 50 % at maximum power.

The APDC enables real time adjustment of drain voltage during operation as a function of the output power, thus providing the SSPA the capability to maintain high efficiency in a wider range of output power level. This is particularly beneficial during power ramps, such as full range current injection or cavities conditioning.

APDC IMPLEMENTATION

Overall scheme of the APDC can be seen in Fig. 1.

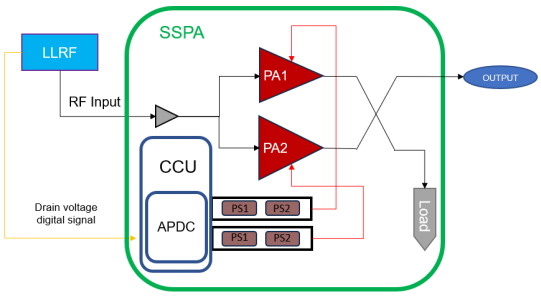

Figure 1: APDC and SSPA block diagram.

There are two operation modes for the APDC:

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- Mode 1: Users set the desired voltage of the PA via the control system using the graphical user interface.

- Mode 2: The ALBA DLLRF control system [4] sets the desired voltage as a function of the reference setting.

For Mode 2, the reference is either the cavity voltage where the SSPA is delivering the power to or the forward power of the SSPA if it is sending power to a dummy load. The reference thresholds where the drain voltage is adjusted and changed is defined by the user internally in the DLLRF firmware. These thresholds are selected according to the maximum forward RF power available for each drain voltage.

Communication between the DLLRF system and the APDC is implemented through a 3-bit digital signal implemented in a DB9 connector. The APDC translates the bit values to the corresponding predefined drain voltage levels for the final-stage transistors and sets the internal power supplies according to this values.

The original SSPA firmware for the PA controllers had to be updated in order to be able to control de power supplies voltage during operation and also the ALBA DLLRF had to be modified to perform the APDC functionality to provide the previously mentioned digital signals.

EXPERIMENTAL RESULTS

The two modes were measured in the ALBA RF laboratory. This facility includes all necessary auxiliaries such as DLLRF and the water cooling among others.

Figure 2: COMMTIA SSPA in the ALBA RF laboratory.

Mode 1

The APDC Mode 1 has been tested with a $5\,kW$ water cooled load. The installation can be seen in Fig. 2.

This mode is non-automatic and the user changes the drain voltage using the graphical control interface. Efficiency versus power curves were measured for different drain voltages. The results are shown in Fig. 3.

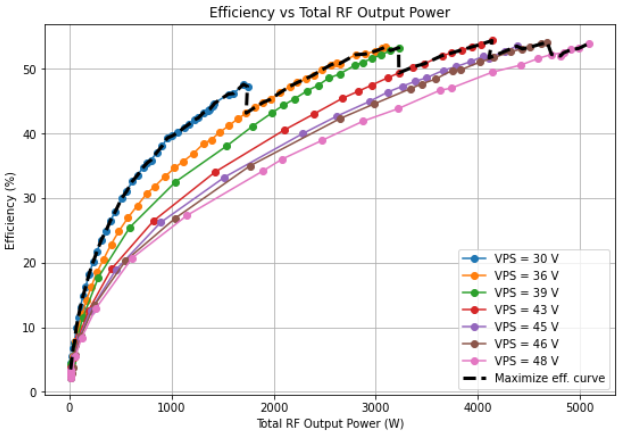

Figure 3: SSPA efficiency over output power in Watts.

The envelope in black shows the maximum achievable efficiency at a given power in the whole SSPA power range.

Mode 2

APDC Mode 2 has been used for the conditioning of the harmonic cavity [5, 6] to be installed at ALBA in the framework of the upgrade of ALBA towards a fourth generation machine [7].

This mode is the automatic supply rail optimization. The DLLRF changes the voltage of the transistors as a function of the reference as it can be seen in Fig. 4

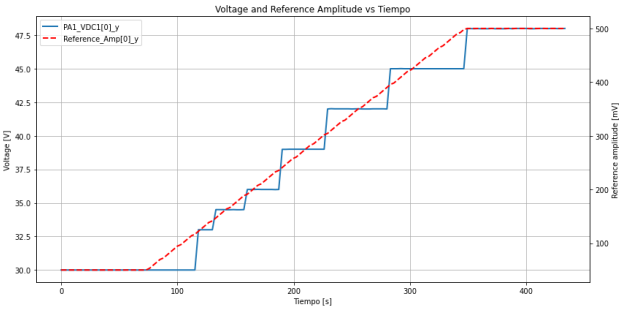

Figure 4: Voltage reference and drain voltage.

The different reference values and digital values of the DLLRF can be adjusted in the firmware and are shown in Table 1.

The results in Table 1 show that the efficiency improvement achieved with the APDC technique depends on the operating power level as expected. The major increase in efficiency is reached at lower output power, where the baseline design did not optimize it.

Table 1: DLLRF input signal, drain voltage, APDC bit values and relative efficiency improvement.

Drain Voltage [V]	DLLRF [mV]	APDC [bit]	Max. output power [W]	$\Delta Eff_{rel.}$ [%]
30	111.2	000	1743.8	38.31
36	143.0	001	3001.9	21.81
39	183.2	010	3224.6	21.44
43	234.0	011	4138.7	9.85
45	300.0	100	4382.8	5.84
46	385.0	101	4681.2	3.55
48	493.0	111	5092.1	—

SSPA Gain Considerations

A consequence of the APDC implementation is the loss of gain at lower voltages. This behavior was expected and measured and it is showed in Fig. 5.

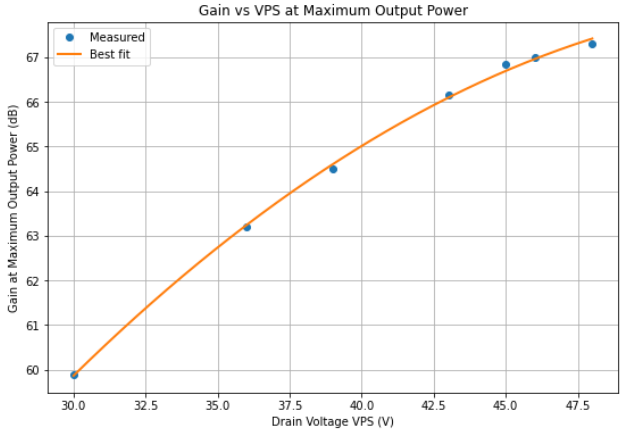

Figure 5: Gain against drain voltage.

As a result, the DLLRF has to send more drive to the amplifier to compensate it. When operated in close loop to the cavity this phenomena is transparent for the user.

CONCLUSION

This contribution presents the APDC as main strategy to improve the efficiency of the 5 kW CW 1.5 GHz SSPA developed by COMMTIA in the framework of the RF2.0 project. The proposed solution relies on a modular and fault-tolerant architecture designed for research facilities RF applications, such as particle accelerators.

This system enables real-time adjustment of the drain voltage during RF operation, allowing the amplifier to operate more efficiently over a larger range of output power levels. The voltage adjustment can be done either manually using the graphical user interface or by defining up to seven different thresholds in the DLLRF in order to automatically change the voltage as a function of the loop reference.

The results obtained during the laboratory measurements show a clear improvement in wall-plug efficiency and are consistent with the one expected during the design phase. These efficiency improvements were achieved without compromising the reliability and fiability of the SSPA.

The results show that APDC strategy can significantly improve the efficiency of the SSPA based RF sources, contribute to the development of more sustainable RF systems and reduce the overall energy consumption of the future accelerator facilities. These improvements support a more sustainable and friendly environmental awareness infrastructures, in line with the broader goals of the RF2.0 initiative.

ACKNOWLEDGMENTS

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