DIGITAL SIGNAL COMPONENT SEPARATOR FOR THE LANL SOLID-STATE POWER AMPLIFIER*

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Abstract

Because of aging, and product discontinuity, LANSCE is investigating the replacement of high power RF amplifiers. A promising candidate is the GaN solid-state power amplifier (SSPA). The outphasing technique provides high efficiency operation of the SSPA. A key element of the outphasing technique is the signal component separator(SCS), which converts an Amplitude Modulation-Phase Modulation(AM-PM) signal to two PM only signals. In this paper, a design of a digital signal component separator (DSCS) in In-phase/Quadrature(I/Q) coordinate is addressed. In addition, the feedback linearizers are proposed to suppress the input disturbances to the SSPA. The DSCS is implemented on the present Field Programmable Gate Array(FPGA) based LANSCE digital low level RF (DLLRF) control system. The performance of the DSCS on the cavity field control system is verified on a low power teststand and the results are reported.

INTRODUCTION

The high power RF amplifiers, klystrons, of LANSCE 805 MHz CCLs have been operating for more than 5 decades. Because of aging, and product discontinuity, LANSCE is investigating the replacement of high power RF amplifiers. One of the highly promising amplifiers are the GaN amplifiers[1]. Currently, an available GaN amplifier can produce 5kW pulsed RF power. Hence, in order to produce the equivalent or better performance than a LANSCE klystron of which peak power is 1.25 MW, a multitude of Solid-State Power Amplifiers are to be combined together. For a high drain voltage, the drain power dissipation is increased as the operating efficiency becomes low[1]. In order to operate a SSPA at high efficiency, the amplifier is operated as close as possible to the 1 dB compression zone or even at the saturation region. The outphasing technique can provide this requirement of the SSPA operation[2]. In the outphasing amplifier, the Amplitude Modulation-Phase Modulation(AM-PM) input signal is converted to constant envelope PM signals, so that each amplifier of the forward signal path linearly amplifies constant envelope PM input signals[3,4]. The combiner sums the amplified PM signals, yielding the signal of linear amplification of the outphasing amplifier input signal.

The core part of the outphasing amplifier is the signal component separator(SCS), which converts the AM-PM input signal to constant envelope PM signals. Most SCS techniques are implemented on the analog circuits[3]. In this paper, a digital signal component separator (DSCS) design in the In-phase/Quadrature(I/Q) coordinate is addressed.

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In addition to the DSCS, compensators for the slowly varying amplitude and phase disturbances that may exist on the RF forward paths are addressed. The sources of these disturbances may be the parameter drifts of the amplifiers themselves, droops of DC power source, or temperature variation of the component. In this outphasing amplifier design, digital feedback linearizers are implemented to compensate for these disturbances.

The proposed techniques of DSCS, feedback linearizers are to provide the stable RF power to a plant, accelerator cavity. In this paper, they are designed, implemented and their performances are verified on the low power cavity field control system testbench experiment.

OUTPHASING AMPLIFIER AND DIGITAL SIGNAL COMPONENT SEPARATOR

The phase modulated components are generated using vector decomposition of the baseband signal in I/Q coordinate.

Consider the phasor diagram shown in Figure 1. The input vector $\vec{s}$ can be expressed as the complex form in I/Q coordinate as

$$\vec{s} = re^{j\alpha} = I + jQ \qquad (1)$$
$$|\vec{s}| = r \le r_{max}, \quad \alpha = atan\left({}^{Q}/_{I}\right)$$

When the vector $\vec{s}$ is projected to the circle of the radius of r_{max} the projecting vector is defined by

$$\vec{e} = e_I + je_Q \qquad (2)$$
$$e_I = -\sin(\alpha)\sqrt{r_{max}^2 - r^2}$$
$$e_Q = +\cos(\alpha)\sqrt{r_{max}^2 - r^2}$$

and the two signals of two-port SCS are given by

$$\vec{d}_0 = r_d\, e^{j(\alpha+\theta)} = I_{d0} + jQ_{d0} \qquad (3)$$
$$\vec{d}_1 = r_d\, e^{j(\alpha-\theta)} = I_{d1} + jQ_{d1} \qquad (4)$$

where

$$\theta = \text{atan}\left(\frac{\sqrt{r_{max}^2 - r^2}}{r}\right)$$

$$I_{d0} = I + e_I, \quad Q_{d0} = Q + e_Q$$
$$I_{d1} = I - e_I, \quad Q_{d1} = Q - e_Q$$

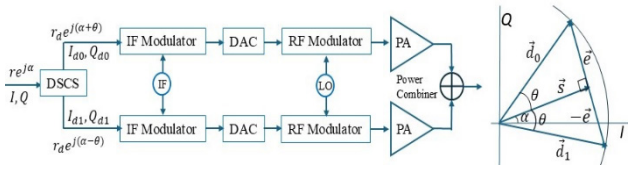

Figure 1: Two-port DSCS outphasing amplifier schematic and vector diagram.

The two-port SCS and the IF modulators are implemented on the LANSCE DLLRF control system. For the IF modulators, the Intel FPGA NCO (numerically controlled oscillator) IP is used to generate 25.15625MHz IF signal. For the RF modulators, an analog front end of the LANSCE low level RF system is used with a 776.84375MHz Lo generator[5]. CORDICs(COordinate Rotation Digital Computer) are implemented on the FPGA to convert the amplitude/phase to the I/Q vector and vise versa, and calculate the square root.

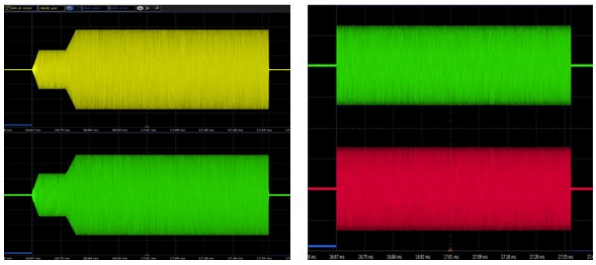

Figure 2: Oscilloscope captured RF waveforms of two-port DSCS outphasing amplifier. (top left) AM-PM DSCS input signal; (bottom left) Combiner output signal; (top right, bottom right) two RF modulation signals of the DSCS outputs.

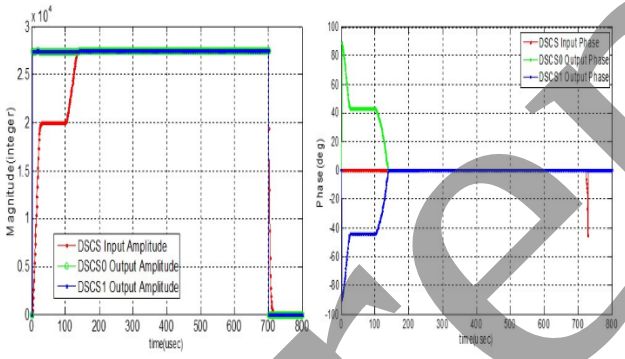

Figure 3: Baseband Signals captured by Quartus II SignalTap II Logic Analyzer. (left) DSCS input/output amplitudes. (right) DSCS input/output phases.

Figure 2 shows the oscilloscope captured RF signals of the two-port DSCS outphasing amplifier. The combiner constructs the AM-PM RF signal that has the same shape of the AM-PM RF signal of the DSCS input. The RF modulation signals of the baseband DSCS outputs are constant envelope PM signals, which drive the power amplifiers of each signal forward path. Figure 3 shows the baseband signals of DSCS inputs and outputs, which show that the varying DSCS input amplitude(red line of left figure) yields the constant amplitude outputs of DSCS and varying phase DSCS outputs(green/blue lines of right figure).

FEEDBACK LINEARIZER

By the DSCS, the AM-PM signal is converted to constant envelope PM signals, which is amplified by the intermediate amplifiers to operate the power amplifiers in their compression zone for high efficiency. This operation leads to nonlinear distortions at the outputs. This issue can be corrected by a linearizer. On the other hand, there exist the both amplitude and phase drifts on the forward path of signals, due to the temperature drift, power supply droop, high power supply ripples, etc. These input disturbances can be suppressed by feedback control. Then, a feedback linearizer provides both the linearization and the input disturbance suppression.

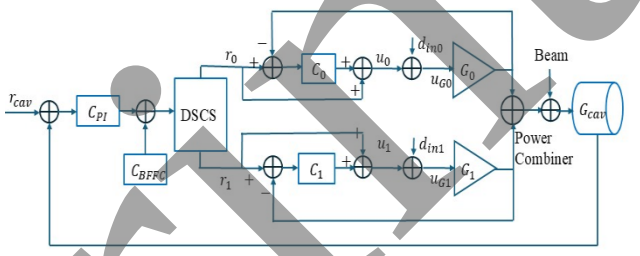

Figure 4: Functional block diagram of the cavity field control system with two-w DSCS based outphasing amplifier and feedback linearizers.

Consider the functional block diagram shown in Fig. 4. In Figure 4, r_0, r_1 are 2-dimensional I/Q vector outputs of DSCS, u_0, u_1 are 2-dimensional I/Q vector outputs of the feedback linearizers, d_{in0}, d_{in1} are 2-dimensional I/Q vector of unknown input disturbances, and G_0, G_1 are 2-by-2 diagonal transfer matrices of the power amplifiers in I/Q coordinate. Also, C_{PI} is a PI feedback cavity field controller and C_{BFFC} is a beam feedforward controller. The possible cross-couplings in the I/Q coordinate power amplifiers are lumped to the input disturbances d_{in0}, d_{in1}.

The output u_0 of the feedback linearizer C_0 is expressed as

$$u_0 = (I_2 + C_0G_0)^{-1}C_0r_0 - (I_2 + C_0G_0)^{-1}C_0G_0d_{in0}$$

which is approximated as

$$u_0 \approx G_0^{-1}r_0 - d_{in0} \qquad (5)$$

by tuning the feedback controller to satisfy $|C_0(\omega)| \gg 1$.

Similarly, the output u_1 of the feedback linearizer C_1 is expressed as

$$u_1 = (I_2 + C_1G_1)^{-1}C_1r_1 - (I_2 + C_1G_1)^{-1}C_1G_1d_{in1}$$

$$u_1 \approx G_1^{-1}r_1 - d_{in1} \qquad (6)$$

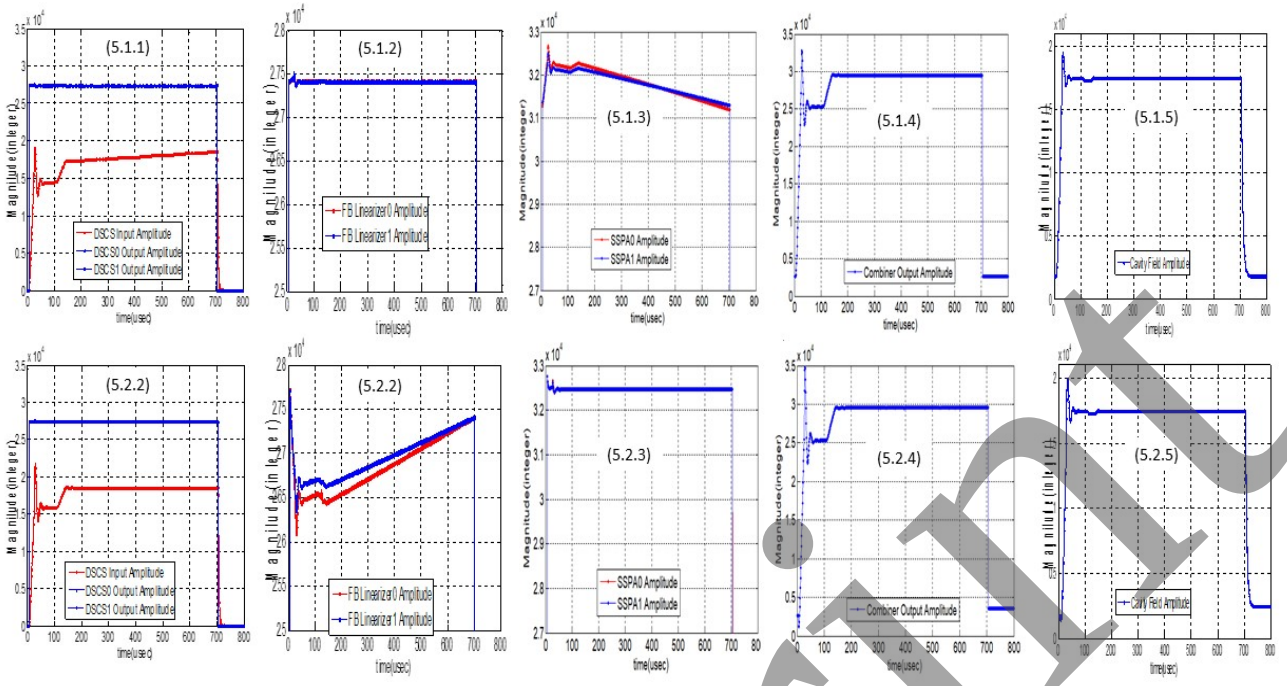

Figure 5: Baseband Signals captured by Intel Quartus II SignalTap II Logic Analyzer.

The feedback linearizers implemented in this paper are of Proportional-Integral(PI) type. Since the input disturbances are slowly varying, by a proper tuning of the PI controller gains, $|C_0(\omega)| \gg 1$ and $|C_1(\omega)| \gg 1$ are achieved at low frequency and so (5), (6) are archived. Note that in (5) and (6), u_0 and u_1 include unknown disturbances d_{in0}, d_{in1}. Applying (5) and (6), for , the approximations of the amplifier inputs u_{G0}, u_{G1} are obtained.

$$u_{G0} \approx G_0^{-1} r_0 \quad (7)$$

$$u_{G1} \approx G_1^{-1} r_1 \quad (8)$$

Since r_0, r_1 are baseband DSCS output I/Q signals and their amplitudes are constants, the amplitudes of the driving RF signals of the amplifiers are constant.

Figure 5 shows the DSCS and feedback linearizer performance experimental results for the amplitude droop compensation tested on the low power cavity field control system testbench. Figure 5.1.(1-5) are the case when feedback Linearizers are Disabled and Fig. 5.2.(1-5) are the case when feedback Linearizers are Enabled. The power droop measured at the SSA testbench is 14% when the RF pulse width is 1.0 msec[6]. For the linearizer performance test with 700usec RF pulse, the droops of each branch amplifiers as 10% and 8%, respectively. Figure 5.1.1 shows that the cavity field feedback controller(DSCS input) compensates for the amplitude when the feedback linearizers are OFF. In contrast, when the feedback linearizers are ON, as shown in Fig. 5.2.2, the feedback linearizers locally compensate for the decreasing amplitude droops on the SSPAs and the effects of the droops are not observed on the cavity field feedback controller output(Fig. 5.2.1). In both cases, the DSCSs work well. When the feedback linearizers are OFF, the SSPAs are driven by the constant DSCS outputs(Fig. 5.1.2) and the effects of the amplitude droops in SSPAs are observed at the SSPA outputs(Fig. 5.1.3). These droops are fedback to the cavity field controller and compensated(Fig. 5.1.1). When the feedback linearizers are ON, the feedback linearizers implicitly estimate the amplitude droops on SSPAs and the estimates are summed to the DSCS outputs yielding the SSPA drive inputs (Fig. 5.2.2) making the SSPA operating at the constant amplitudes close to the saturation region(Fig. 5.2.3), where the operating point of SSPAs can be set by the variable gain Pre-Amplifiers. Whether the feedback linearizers are Disabled (Fig. 5.1.(1-5)) or Enabled (Fig. 5.2.(1-5)), or, whether the amplitude droops in SSPAs are compensated by the cavity field feedback controller or by the local feedback linearizers, the effects of the amplitude droops on SSPAs are not observed in the Combiner output(Fig. 5.1.4 and Fig. 5.2.4) and the cavity field output (Fig. 5.1.5 and Fig. 5.2.5).

SUMMARY

In this paper, a FPGA implementation of the two-port signal component separator (SCS) which can be easily extended to four-port, eight-port DSCS is addressed. On the other hand, the digital PI feedback linearizers are implemented to suppress the amplitude and phase droops and possible slowly varying external disturbance inputs to a SSPA. The performances of the DSCSs and the feedback linearizers are verified by integrating them to the low power cavity field control system testbench.

REFERENCES

[1] J. Lyles *et al.*, "High Power GaN Amplifier Development for Coupled Cavity Linac at LANSCE", presented at the IPAC'26, Deauville, France, May 2026, paper TUP7347, this conference.

[2] H. Chireix, “High Power Outphasing Modulation,” *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935. doi:10.1109/jrproc.1935.227299

[3] T. W. Barton and D. J. Perreault, “Theory and Implementation of RF-Input Outphasing Power Amplification,” IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 12, pp. 4273–4283, Dec. 2015. doi:10.1109/tmtt.2015.2495358

[4] Ying Tian, Q. Hammi, S. Boumaiza, and F. M.Ghannouchi, “Design and Optimization of Digital Signal Components Separator of LINAC Transmitters Using FPGA Processors,” in *Proc. ICSPC’2007*, pp. 836-839, Dubai, UAE, Nov. 2007. doi:10.1109/icspc.2007.4728449

[5] S. Kwon *et al.*, “FPGA Implementation of a Control System for the LANSCE Accelerator”, in *Proc. IPAC'16*, Busan, Korea, May 2016, pp. 2771-2773. doi:10.18429/JACoW-IPAC2016-WEPOR044

[6] J. T. M. Lyles, personal communication, April, 2026.