DEVELOPMENT OF FAST ORBIT FEEDBACK SYSTEM AT HALF STORAGE RING *

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Abstract

A distributed Fast Orbit FeedBack system (FOFB) is designed at the Hefei Advanced Light Facility (HALF) storage ring. The system controls the beam orbit instability of the storage ring to the submicron level, by BPM, feedback algorithm and actuator to achieve feedback correction of beam orbit. This paper presents the design of the FOFB system of HALF, including open-loop test results.

INTRODUCTION

The Hefei Advanced Light Facility is a fourth-generation storage ring light source. The storage ring has an electron energy of 2.2 GeV, a natural beam emittance of about 86 pm·rad and an operating beam current of 350 mA. The 480 m storage ring is adopted 20 cells of H6BA lattice structure, with 12 BPM and 4 fast corrector magnets in each cell [1]. The closed-loop design bandwidth of FOFB is 500 Hz, and the frequency of FA is 20 kHz.

The fast orbit feedback system includes three subsystems: beam position measurement, feedback controller, and fast correction actuator. Beam position monitors (BPMs) measure the beam-induced voltage signal, and DBPM processors perform high-speed synchronous ADC sampling on the beam signal to extract turn-by-turn (TBT) and FA beam orbit data. The feedback controller collects beam orbit data at different locations in the storage ring and calculates the beam orbit correction values through a feedback algorithm. The fast correction actuator includes fast corrector power supplies, fast corrector magnets, and the vacuum chamber. The beam orbit is stabilized by changing the magnetic field strength through fast corrector magnets.

Table 1: Main parameters of the HALF storage ring

parameter	**value**
energy	2.2 GeV
circumference	479.86 m
number of cells	20
natural emittance	86.3 pm·rad
transverse tunes (H/V)	48.15/17.15
natural chromaticities (H/V)	−77/−57
energy loss per turn	186.7 keV
momentum compaction factor	9.0×10^{-5}
natural energy spread	0.62×10^{-3}
total absolute bending angle	442.5°
harmonic number (500 MHz RF cavity)	800

II. THE FAST ORBIT FEEDBACK SYSTEM OF HALF

Based on the structural characteristics of the HALF storage ring, 10 beam instrumentation stations are distributed, as shown in Fig. 1. One FOFB processor is installed at each station, connected to 8 local DBPM processors and 16 fast corrector power supplies. Used to process 160 FA data (vertical and horizontal direction for each BPM), and output 160 current setting values corresponding to 80 correction amounts of fast corrector magnets. The FOFB processors are connected via optical fibers to form a bidirectional ring link. The DBPM processors and fast corrector power supplies are connected with local FOFB processor via optical fibers to form a point-to-point link [2].

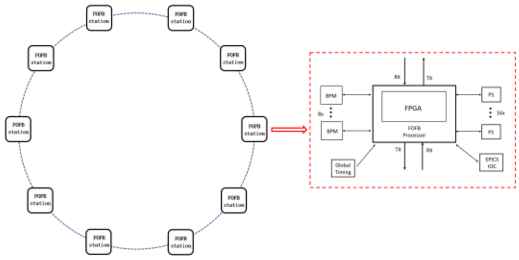

Figure 1: FOFB architecture of HALF.

the HALF fast orbit feedback system adopts an FPGA-based design architecture, as shown in Fig. 2. The fast feedback processor primarily consists of an FPGA chipset, functional components, and external interfaces. The FPGA chipset includes Xilinx Ultrascale+ XVCU9P and Zynq XC7Z020. The former incorporates DSPs for high-performance data and logic operations, with 104 GTY channels for high-speed data transmission; the latter is utilized for system configuration and EPICS software development based on Petalinux. The processor is designed with a 4GB DDR4 data cache space for system state analysis. In terms of external interfaces, it features 10 sets of QSFP connected to FPGA GTY Quad, enabling high-speed optical fiber communication. Additionally, the processor supports external synchronous clock and external trigger signal inputs, as well as Gigabit Ethernet communication.

The processor chassis adopts 1U standard structure and supports FMC expansion interfaces. It can obtain timing information by connecting WR timing sub-board, for generating timestamps of system real-time data.

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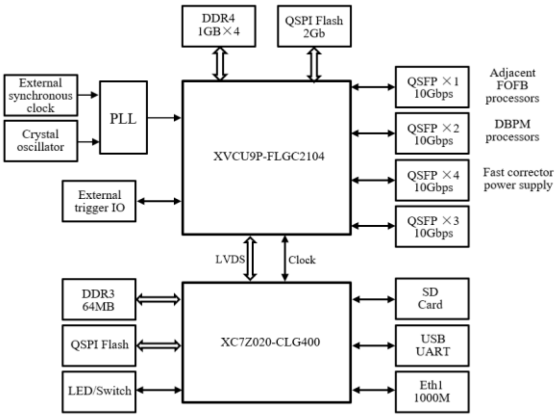

Figure 2: The architecture of FOFB processor.

Figure 3: HALF FOFB processor.

The data processing of FOFB system adopts pipeline grouping operation design to reduce the calculation resource utilization of data operation and overall data processing latency. By dividing the 16 BPM data collected by 8 local DBPM processors into one group, the system can perform calculations while transmitting global data. The matrix used in each calculation process can be simplified into a 16 row and 16 column inverse response submatrix. In order to optimize system performance, this scheme designs a PID control algorithm for all BPM data, before inverse matrix multiplication operation [3].

$$u(k) = u(k-1) + K_p[\Delta x(k) - \Delta x(k-1)] + K_i\Delta x(k)$$

$$+K_d[\Delta x(k) - 2\Delta x(k-1) + \Delta x(k-2)]. \tag{1}$$

$$\begin{bmatrix} r_{1,1} & r_{1,2} & \cdots & r_{1,16} \\ r_{2,1} & r_{2,2} & \cdots & r_{2,16} \\ \vdots & \vdots & \ddots & \vdots \\ r_{16,1} & r_{2,1} & \cdots & r_{16,16} \end{bmatrix}_i \times \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_{16} \end{bmatrix}_i = \begin{bmatrix} \Delta I_1 \\ \Delta I_2 \\ \vdots \\ \Delta I_{16} \end{bmatrix}_i . \tag{2}$$

$$\begin{bmatrix} \Delta\theta_1 \\ \Delta\theta_2 \\ \vdots \\ \Delta\theta_{16} \end{bmatrix} = \sum_{i=1}^{n} \begin{bmatrix} \kappa_1\Delta I_1 \\ \kappa_2\Delta I_2 \\ \vdots \\ \kappa_{16}\Delta I_{16} \end{bmatrix}_i . \tag{3}$$

In PID operation, k is the number of timed cycles. And in the inverse matrix operation, i is the number of data sets, n = 10.

The feedback algorithm of the fast orbit feedback processor mainly includes the following parts. The FOFB processer receives local BPM data, caches and encodes it to form global data. The FOFB processer sends local BPM data to the bidirectional global ring link, receives global data sent by other station. The system writes BPM data and operation parameters into the memory. Data operation adopts pipeline design, grouping data for operation (16 data per group, a total of 10 groups), minimizing feedback delay as much as possible. Accumulate 10 sets of data operation results to obtain 16 local fast corrector power supply setting values, and output them uniformly at a determined time during the synchronous working cycle [4]. The processor stores local BPM data and execution values read back from the fast corrector power supply in DDR4 and uploads it to the control system through EPICS.

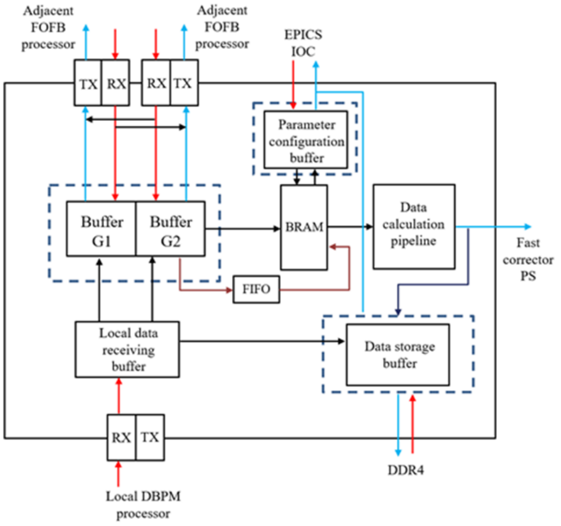

Figure 4: The algorithm of Data processing.

III. THE OPEN-LOOP RESPONSE OF THE SYSTEM

In order to test the open-loop response of the system, we construct a verification testing platform consisting of beam position measurement, distributed controller and fast correction execution device.

We use an arbitrary waveform generator to generate beam simulated signals, which is processed by a DBPM processor algorithm to generate FA data. The FOFB processor is connected to the DBPM processor and the fast corrector power supply via optical fibers, and simulates global data transmission through a self-loop optical fiber link. The fast correction execution device includes a fast corrector power supply, magnet [5], vacuum chamber, and internal magnetic induction coil. An oscilloscope is used to collect current signals, magnetic induction voltage signals, and synchronous trigger signals.

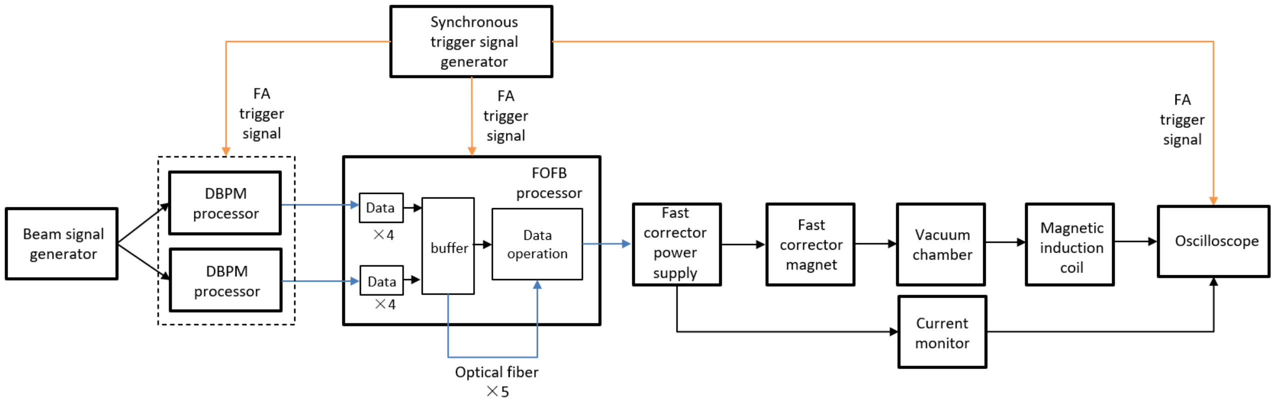

Figure 5: The architecture of open-loop testing platform.

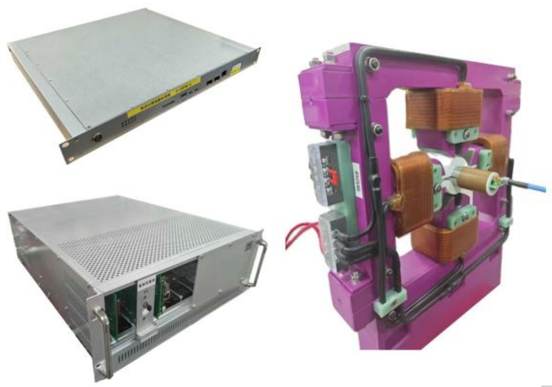

Figure 6: The DBPM processor, fast corrector power supply, and fast corrector magnet.

The BPM electronics delay test method is shown in Fig. 7. A 499.8 MHz sine wave is generated by an arbitrary waveform generator and split into two signals. One path is connected to an oscilloscope, while the other is connected to one of the channels of the DBPM system. The other three inputs of the DBPM are directly fed with sine signals generated by a RF signal generator. After the four signals are sent to the DBPM system, FA data is obtained through pipeline computation. To accurately measure the system delay corresponding to the group delay, a trigger signal synchronized with 20 kHz is sent by the FPGA to control the arbitrary waveform generator to output a sine wave signal mixed with a delayed low-frequency square wave, simulating a sudden change in beam position. When the arbitrary waveform generator outputs the mixed signal to the oscilloscope, the position of the sudden change in the mixed signal is recorded as the start signal. In FA mode, when the difference between two adjacent positions exceeds a threshold, the DBPM processor outputs a pulse signal to the oscilloscope as the stop signal. The BPM electronics delay can be obtained by calculating the delay difference between the stop signal and the start signal. After testing, the BPM electronics delay T_{BPM} is less than 75 µs.

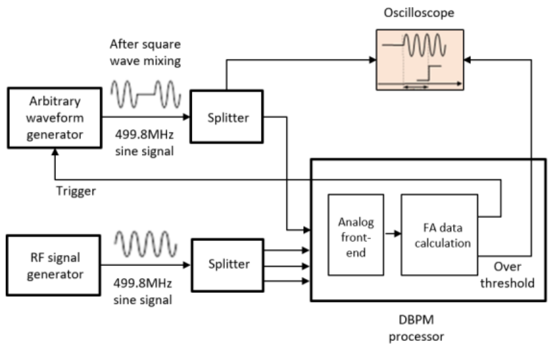

Figure 7: Test of BPM electronic delay.

As shown in Fig. 8, the FOFB processor delay consists of the following components, T_1 local data transmission delay, T_2 data encoding fanout delay, T_3 global data transmission delay, T_4 local data operation delay, T_5 global data operation delay, and T_6 fast corrector power supply data transmission delay.

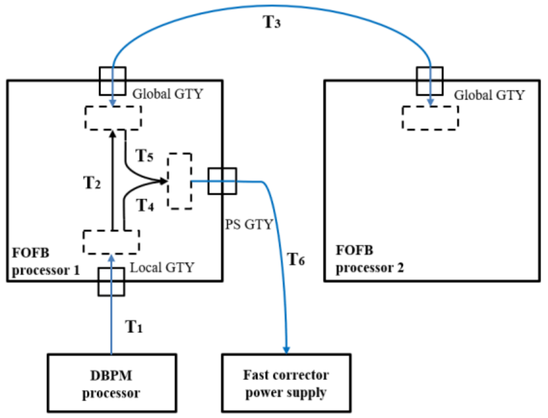

Figure 8: Test of FOFB processor delay.

In the test system, the data transmission link is established using OM3 850 nm multimode optical fiber. The local BPM data are collected by 8 channels through 30 m optical fibers. The global BPM data transmission is tested through 100 m loopback optical fiber to simulate data transmission delay between the two adjacent sub-stations.

PS settings are transmitted through 50 m optical fibers. Integrated logic analyzer (ILA) in the FPGA is used to measure the delays with an accuracy 8 ns for the 125 MHz clock source.

Table 2: The delay of feedback algorithm

	Delay	Fiber Length
T_1	720 ns	30 m
T_2	184 ns	—
T_3	992 ns	100 m
T_4	560 ns	—
T_5	640 ns	—
T_6	840 ns	50 m

The total delay of FOFB processor T_{FOFB} is less than 10 µs.

$$T_{FOFB} = T_1 + T_2 + 5T_3 + T_5 + T_6 = 7344\, ns. \quad (4)$$

The FOFB processor receives synchronous trigger signals and outputs current settings after a delay of 128 ns. The magnetic response (coil induced voltage) of the following current values (±1 mA, ±5 mA, ±10 mA, ±50 mA, ±100 mA, ±0.5 A, ±1 A) is collected through an oscilloscope and integrated to obtain magnetic flux. The Inconel section of the vacuum chamber is 70 mm long and can transmit most of the magnetic field. The power supply response parameters are adjusted to ensure that the magnetic flux curve does not overshoot. And the rise time is taken as the moment when the magnetic flux reaches 90% of its maximum value, as shown in Fig. 9 and Fig. 10. We obtain the fast correction actuator delay.

Table 3: The delay of fast correction actuator

ΔI	Delay
0.002 A (±1 mA)	50.4 µs
0.01 A (±5 mA)	56.1 µs
0.02 A (±10 mA)	56.4 µs
0.1 A (±50 mA)	59.9 µs
0.2 A(±100 mA)	60.9 µs
1 A(±0.5 A)	70.9 µs
2 A (±1 A)	72.3 µs

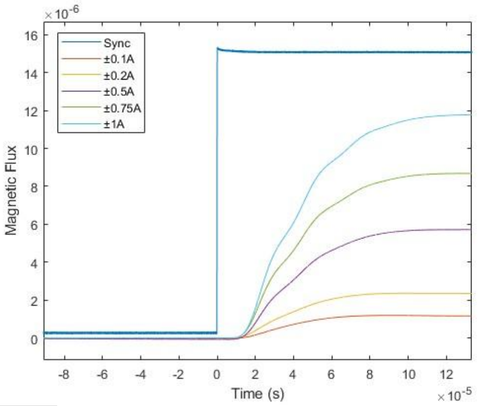

Figure 9: Magnetic flux response, when ΔI ≥0.2A.

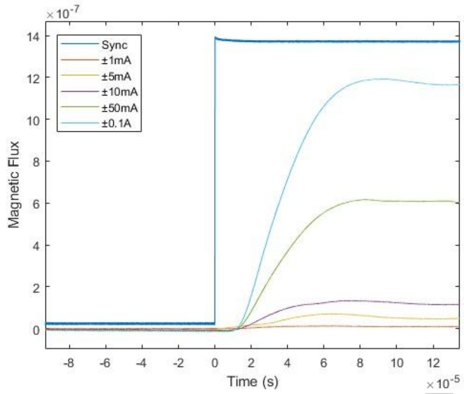

Figure 10: Magnetic flux response, when ΔI ≤0.2A.

Using the rising edge of the trigger signal as a reference, the fast correction actuator delay $T_{correction}$ is less than 75 µs. And the open-loop delay of the system $T_{openloop}$ is calculated by the following formula.

$$T_{openloop} = T_{BPM} + T_{FOFB} + T_{correction} < 160\, \mu s. \quad (5)$$

CONCLUSION

In response to the design requirements of the FOFB system for the HALF storage ring, this paper proposes an FPGA-based architecture for the fast orbit feedback system of the Hefei Advanced Light Facility. We have independently developed FOFB processor and established a system verification platform for open-loop testing. After testing, the system open-loop delay is less than 160 µs, meeting the 500 Hz closed-loop bandwidth.

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