DEVELOPMENT OF A LOW LEVEL RF SYSTEM FOR THE SIRIUS PASSIVE 3rd-HARMONIC CAVITY BASED ON MTCA.4 PLATFORM

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Abstract

The SIRIUS storage ring RF system currently operates with two 500 MHz superconducting cavities, each powered by a 130 kW RF plant composed of two solid-state amplifiers (SSA) and a 200 mA stored beam current. A passive 2-cell superconducting 3rd-harmonic cavity (3HC) is planned for installation in 2027 to increase beam lifetime through bunch lengthening and and increase the stored beam current to the nominal value of 350 mA. This paper presents the current status of the development of a Low Level RF (LLRF) system for the 3HC based on MTCA.4 platform. The system includes a dedicated analog front-end for RF signal acquisition and conditioning, as well as clock and local oscillator (LO) generation. The digital hardware is based on Struck MTCA modules and an additional digital front-end for external signal isolation and interface with the FPGA GPIOs. Finally, the proposed DSP chain for the cavity signal processing and control is presented and discussed.

INTRODUCTION

The SIRIUS storage ring RF system currently operates with two 500 MHz CESR-B type superconducting cavities, each powered by a 130 kW RF plant composed of two solid-state amplifiers (SSA) and a 200 mA stored beam current. A passive 2-cell superconducting 3rd-harmonic cavity designed by SARI (Shanghai Advanced Research Institute) is scheduled for installation in 2027. The objective of this upgrade is to increase beam lifetime by reducing the bunch length [1–3] and increase the stored beam current to the nominal value of 350 mA.

This report presents the current status of the development of a Low Level RF (LLRF) system for the passive 2-cell superconducting 3rd-harmonic cavity, based on a commercial off-the-shelf (COTS) MTCA.4 platform. The final design of the analog front-end, including clock and local oscillator (LO) generation, is described, as well as the digital front-end for signal conditioning and interface with Struck MTCA modules. The intended DSP chain is also discussed.

GOALS AND REQUIREMENTS

The main parameters and stability requirements for the SIRIUS 3rd-harmonic cavity are presented in Table 1.

The voltage in a passive harmonic cavity can be expressed as [4]:

Table 1: Main Parameters of the 3rd-harmonic Cavity

Parameters	Value	Unit
n	3	-
f_{rf}	499.687	MHz
f_{hrf}	1499.001	MHz
R/Q (π mode)	<90	Ω
R/Q (0 mode)	<0.2	Ω
Q (π mode)	$> 2 \cdot 10^8$	-
Nominal Beam Current	350	mA
Harmonic Voltage Stability	$< \pm 0.2$	%
Nominal Harmonic Voltage	1	MV

$$V_b \approx -I_{dc} \frac{R_s}{Q} \frac{f_{hrf}}{\Delta f} \cos\left(n \cdot 2\pi f_{rf} \cdot \tau - \psi_h\right), \quad (1)$$

where I_{dc} is the beam current, R_s and Q are respectively the shunt impedance and quality factor of the cavity π-mode, f_{hrf} is the harmonic cavity resonance frequency, f_{rf} is the fundamental RF frequency, ψ_h is the harmonic cavity detuning angle, n is the harmonic number, and $\Delta f = f_{hrf} - n f_{rf}$ is the harmonic cavity detuning frequency. The relationship between the detuning angle ψ_h and the detuning frequency is given by:

$$\tan \psi_h = 2Q \frac{\Delta f}{f_{hrf}}. \quad (2)$$

The control system aims to keep the harmonic voltage amplitude constant ($|V_b| \approx I_{dc} \frac{R_s}{Q} \frac{f_{hrf}}{|\Delta f|}$). As shown in Eq. (1), the voltage fundamentally depends on the cavity detuning, allowing V_b to be controlled by adjusting its resonance.

According to the data in Table 1 and Eq. (1), the operational detuning is determined to be $\Delta f \approx 45$kHz. To meet the voltage stability requirement, the tuning stability must achieve a minimum of 90 Hz.

LLRF MAIN MODULES

The tuning system consists of an analog front-end for conditioning the cavity and its control signals; a digital front-end responsible for conditioning and interfacing digital signals with the FPGA hardware; an MTCA Rear Transition Module (RTM) for downconversion; and an MTCA Advanced Mezzanine Card (AMC) for digitization and FPGA-based digital signal processing (DSP). The mechanical actuators for the cavity tuner are composed of a stepper motor for coarse tuning and a piezoelectric for fine tuning. Figure 1 presents the general block diagram of the system. The details of these

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blocks and their interconnections will be further discussed in the following sections.

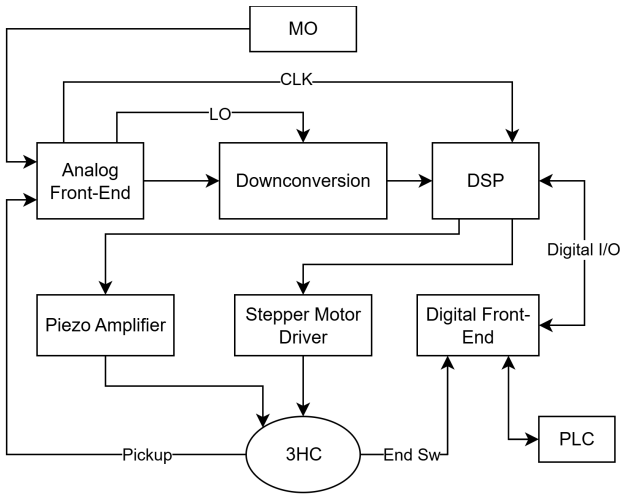

Figure 1: General block diagram of the system.

MTCA Solutions

The MTCA.4 platform was chosen for the LLRF to standardize with other SIRIUS systems, such as the LINAC LLRF, BPM Digitizers, and FOFB LLRFs [5–7]. The project is based on the SARI LLRF [8] due to similarities between the facilities.

MTCA modules from Struck are widely adopted by other facilities as commercial solutions in LLRF systems. For this project, the RTM DWC8VM1 [9] and the AMC SIS8300KU [10] will be employed in a NATIVE-R2 MTCA.4 [11] crate.

The DWC8VM1 is a downconversion RTM with eight AC-coupled channels with a 700-4000 MHz bandwidth, as well as digitally programmable attenuators up to 30 dB. It also features two DC-coupled inputs, operating from DC to 650 MHz, and a maximum voltage of 2 V_{pp}.

The SIS8300KU is a digitizer AMC with two output DACs (−1 to 1 V output) and two RJ45 connectors for IO communication, one with four differential digital inputs and another with four differential outputs. To interface with the digital IO, a digital front-end is required to convert external signals, such as end switches (dry contact) and interlocks (dry contact and TTL), to the differential standard, as well as to perform the inverse conversion for the outputs.

DSP

The project aims to develop an open-source FPGA firmware with top-level simulability, and the proposed DSP chain diagram is shown in Fig. 2. The code is currently under development, and the hardware validation is planned for the second half of 2026.

The analog signals are I/Q sampled and decimated by a CIC (Cascade Integrator-Comb) filter. A rotation block applies gain and phase adjustments for the control loop compensation. Next, the signals are converted from rectangular to polar by the CORDIC (Coordinate Rotation Digital Computer) block. The amplitude of the pickup signal is the main control parameter.

A reference signal for the stored beam current is used to define the operating control loop mode: low gap voltage at low current, fixed detune for intermediate values, and fixed gap voltage for currents near nominal value. The control loop will keep the cavity detuning fixed during the beam current ramp, thus minimizing continuous piezo operation, reducing premature wear of the piezo and preventing mechanical stress on the cavity.

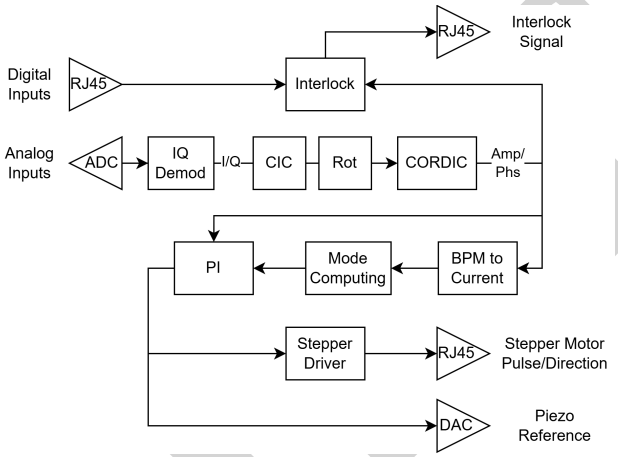

Figure 2: DSP block diagram.

ANALOG FRONT-END

The Analog Front-End comprises three main modules for the LLRF operation: the Clock Generation, the Pre Front-End, and the BPM Distribution.

Clock Generation

The clock generation block generates the clock signal for the FPGA and the LO for the downconverter from the master oscillator (MO).

The clock frequency selected for SIS8300KU operation is 125 MHz. To enable I/Q sampling, the intermediate frequency is set as $f_{if} = f_{clk}/4 = 31.25$ MHz, resulting in a LO frequency $f_{LO} = f_{hrf} - f_{if}$. Figure 3 shows the block diagram of the LO and clock signal generation.

Frequency division is performed using the digital synthesizer Valon 3010a [12], while multiplication is carried out by the Mini-Circuits multiplier FK-3000+ [13].

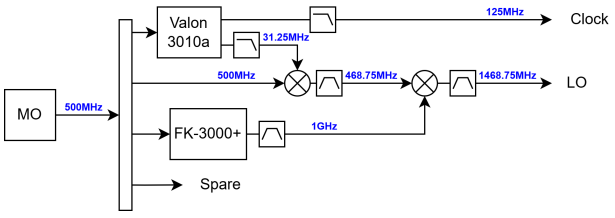

Figure 3: Block diagram of the clock and LO generation crate.

Pre Front-End

The main function of the Pre Front-End is to condition the analog signals for the DWC8VM1 downconversion RTM. The cavity pickup signal is connected to RF couplers to provide additional monitoring signals and attenuators can be connected if needed. The signal from the BPM is up-converted to the RF frequency, enabling proper processing by the DWC8VM1.

Additionally, the load leveler of the 3HC cryomodule requires a DC voltage signal proportional to the cavity field. This signal is provided by the Mini-Circuits RF Power Sensor ZX47-40LN-S+ [14] in the Pre Front-End crate.

Beam Position Monitor Signal Distribution

A reference signal for the stored beam current is needed in the LLRF to switch between operating modes. A BPM signal, which was already available from diagnostics systems, was chosen for this project and shown to be proportional to DC mean beam current. Although this measurement is available from the DC Current Transformer (DCCT) sensor, the distance between the installed DCCTs and the LLRF system cabinet makes physical cabling unfeasible, and the monitoring data from EPICS would rely on the communication network availability.

Figure 4 shows a block diagram from the BPM signal source to the distribution crate. A stripline BPM is connected to a Dimtel hybrid BPMH-20-2G [15], which provides a sum output port that is available through cable in the RF room. Then, this signal is filtered by a pass-band filter with center frequency of f_{rf}, amplified and divided to provide three additional signals for other systems.

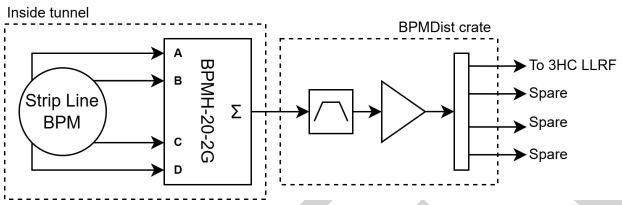

Figure 4: Block diagram of the BPM distribution crate.

PIEZO AND MOTOR DRIVER

For coarse tuning, the system employs the RKSD507M-C stepper motor driver by Oriental Motors [16], which receives digital pulse and direction signals from the digital front-end.

Fine tuning is achieved using a piezo actuator driven by a PI E-470 series controller [17]. This amplifier provides an output range of 0 to 1000 V with input signals from 0 to 10 V. Since the SIS8300KU DAC outputs ranges from −1 to 1 V, an additional amplification stage is needed. A low-noise amplifier developed at LNLS for light source applications will be used to match the DAC output to the controller input.

The overall tuning range is ±500kHz, with the fine tuning range provided by the piezo actuator being 20kHz [18].

DIGITAL FRONT-END

The digital interface of the SIS8300KU consists of an RJ45 connector with four differential digital inputs and another RJ45 with four differential digital outputs. The LLRF system interacts with a variety of devices, such as end switches, external interlocks, and stepper motor direction and pulse signals, which requires an interface that supports different signal standards, including dry contact, TTL, and LVTTL.

Therefore, a dedicated printed circuit board (PCB), shown in Fig. 5 was developed for signal interfacing with the SIS8300KU. This board converts signals from innumerous sources to the differential standard required by the SIS8300KU, ensuring both electrical isolation and signal integrity. The PCB provides seven input channels: two for end switches, one for trigger input, and four interconnected channels for external interlock. It also provides seven output channels, including pulse and direction for the stepper motor, a trigger output, and four interconnected channels for interlock.

Channel isolation is achieved using optocouplers. Additionally, the outputs can be configured as either dry contact or TTL by internal jumpers, providing flexibility for different applications.

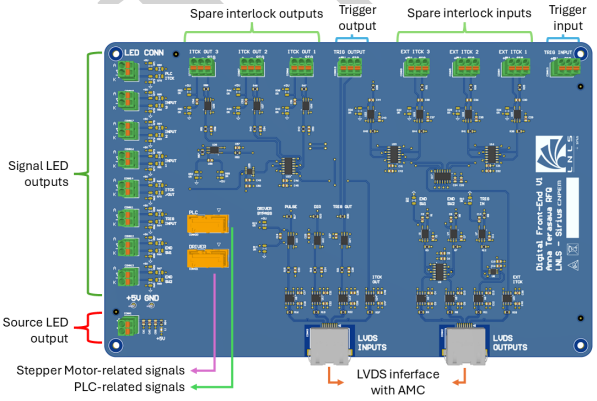

Figure 5: Digital Front-End PCB.

CONCLUSION

This paper presented the conceptual design and ongoing development of the LLRF system for the passive 3HC at SIRIUS. The proposed architecture is based on MTCA.4 to ensure compatibility, reliability, and ease of integration with existing systems. The dedicated analog and digital front-ends, as well as the DSP chain, were detailed to address the specific requirements of the application.

The project is currently in the development phase, with functional tests scheduled for the second half of 2026 and installation of the 3HC planned for 2027. Future work also includes integration with software applications and EPICS IOC development for control and monitoring of the system.

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