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Development of BPM electronics for PIP-II at Fermilab

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PIP-II (Proton Improvement Plan-II) is a critical upgrade to the Fermilab accelerator complex. The 800 MeV superconducting linear accelerator will utilize 126 beam position monitors (BPMs) across the Warm Front End (WFE), superconducting linac (SC LINAC), and Beam Transfer Line (BTL). These BPMs provide beam position, phase, timing, and intensity data, meeting stringent physics requirements: 10 μm position resolution, 0.1 mm position accuracy, 1% intensity resolution, 0.3° phase resolution, and 1° phase stability. This paper presents the uTCA4.0-based BPM electronics system. Each AMC with an RTM processes eight signals from two BPMs, with a 12-slot uTCA chassis supporting up to 24 BPMs. The system features 8-channel 250 MSPS ADCs and a Xilinx UltraScale+ SoC FPGA running Linux, facilitating high-speed data transfer via 10 Gigabit Ethernet. Key design aspects include analog signal conditioning, JESD204B routing, clock distribution, and thermal management. FPGA handles BPM signal processing, time tag, digital down-conversion, and phase drift compensation. Performance benchmarks, including position, phase resolution and temperature stability, are validated through dedicated testing.

Footnotes

Funding Agency

I have read and accept the Conference Policies

Yes

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