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Optimization and Upgrade of the BPM Electronics System for CSNS-II RCS

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As the China Spallation Neutron Source (CSNS) Phase II project increases the Rapid Cycling Synchrotron (RCS) power to 500 kW, the signal intensity of Beam Position Monitors (BPMs) is expected to rise tenfold, necessitating a comprehensive upgrade of the electronics system to meet high-power operational requirements. Drawing on the experience of the J-PARC Main Ring (MR) 1.3 MW power upgrade, CSNS optimized the analog front-end using a MicroTCA-based RTM board. The initial four-stage passive resistive divider was upgraded to a switchable attenuator combined with proportional voltage division, alongside impedance matching techniques, ensuring stable signal attenuation under high input voltages, minimal reflections, and compatibility with the Analog-to-Digital Converter (ADC) dynamic range. The digital processing is implemented on a self-developed MicroTCA.4-based AMC board, utilizing the Xilinx Zynq-7045 SoC with 8 channels of 16-bit ADC (125 MSPS). The system has successfully transplanted algorithms, supports real-time beam position calculations, and publishes position signals via EPICS. Tests demonstrate low noise, high linearity, and performance.

Footnotes

Funding Agency

I have read and accept the Conference Policies

Yes

Author: QIU, Ruiyang (Institute of High Energy Physics)

Co-authors: LI, Fang (Institute of High Energy Physics); ZENG, Lei (Institute of High Energy Physics); REHMAN, Muhammad Abdul (Institute of High Energy Physics); YANG, Renjun (Institute of High Energy Physics); HUANG, Weiling (Institute of High Energy Physics); CHEN, Weiwen (Institute of High Energy Physics); XU, Zhihong (Institute of High Energy Physics)

Presenter: QIU, Ruiyang (Institute of High Energy Physics)

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