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FELIX, the ATLAS readout system: from LHC Run 3 to Run 4

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After being successfully deployed to read out a subset of the ATLAS detectors during LHC Run 3 (2022-2026), FELIX will serve all ATLAS detectors in LHC Run 4 (2030-2033). FELIX is a router between custom serial links from front-end ASICs and FPGAs to data collection and processing components via a commodity switched network. FELIX is also capable of fixed-latency forwarding the LHC clock, trigger accepts, and resets received from the TTC (Timing, Trigger and Control) system to front-end electronics. FELIX uses FPGA-based PCIe I/O cards installed in commodity servers. To cope with the increased data rate expected after the major upgrade to the LHC and the detector in between runs, the FLX712 Run 3 PCIe Gen3x16 card, based on an AMD Kintex Ultrascale XCKU115 FPGA, will be replaced with the FLX155, a bifurcated 2x PCIe Gen5x8 card equipped with an AMD Versal Premium VP1552 FPGA/SoC. Firmware installed on the FPGA and software running on the FELIX server are also being upgraded to handle the increased data rate.

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Footnotes

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