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## RFSoc based Transverse Feedback Processor for J-PARC Proton Synchrotrons

*Wednesday, October 22, 2025 8:30 AM (30 minutes)*

Transverse feedback suppresses beam instabilities that are prominent in high-intensity beams and is essential for their stable acceleration. At J-PARC, a digital signal processor is being developed for the transverse feedback systems in the Main Ring and RCS proton synchrotrons. The processor uses an RFSoc, an FPGA with integrated ADCs and DACs. It segments 100-ns-long bunches at a sampling rate of 576 MS/s and applies piecewise feedback control to each segment.

The processor performs the following functions:

1) BPM signals with differential response are offset-corrected and integrated to detect the position of each segment. 2) FIR filtering compensates for changes in the revolution period during acceleration. 3) Feedback kick timing is varied to match beam passage timing at the kicker, which changes with the revolution period.

This presentation describes the processor architecture and reports results from bench tests.

### Footnotes

### Funding Agency

### I have read and accept the Privacy Policy Statement

Yes

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