Contribution ID: **712** Contribution code: **THPB056**   Type: **Poster Presentation**

Architecture reconstruction and optimization of front-end Interlock system in TPS

Thursday 5 June 2025 15:30 (2 hours)

The Taiwan Photon Source's (TPS) Front-End Interlock System has been upgraded to solve operational complexity and maintainability that were noticed in the early stages of operation. For increased dependability and fault-handling capabilities, one of the main enhancements is switching the logic core from an FPGA-based architecture to a fault-tolerant dual-sequential CPU architecture.

The system integrates redundant dual CPUs with shared relay monitoring and adopts a Real-Time Operating System (RTOS) to optimize signal processing. Additionally, the safety functionalities have been restructured to include fail-safe mechanisms, independent loop monitoring, and improved logic for cooling water flow and vacuum monitoring. These updates aim to reduce unnecessary emergency shutdowns and improve system reliability.

While preserving compatibility with the legacy system, this new version streamlines the design, increases diagnostic efficiency, and expedites the deployment process for future upgrades.

Footnotes

Paper preparation format

Region represented

Asia

Funding Agency

Author: HSIAO, Yuan-Ming (National Synchrotron Radiation Research Center)

Co-authors: CHENG, Chia-Mu (National Synchrotron Radiation Research Center); GUO, Yan-Hong (National Synchrotron Radiation Research Center); SHUEH, Chin (National Synchrotron Radiation Research Center); CHENG, Yu Tsun (National Synchrotron Radiation Research Center); CHAN, Che-Kai (National Synchrotron Radiation Research Center); KUAN, Chien-Kuang (National Synchrotron Radiation Research Center); SHENG, I-Ching (National Synchrotron Radiation Research Center); CHANG, Chin-Chun (National Synchrotron Radiation Research Center)

Presenter: HSIAO, Yuan-Ming (National Synchrotron Radiation Research Center)