MACHINE PROTECTION SYSTEM FOR HIAF *

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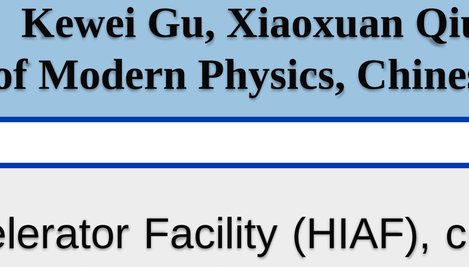
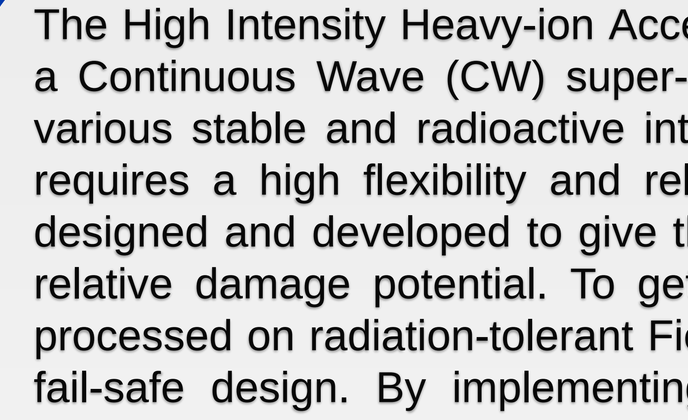
The High Intensity Heavy-ion Accelerator Facility (HIAF), currently under construction, is a complex machine that couples a Continuous Wave (CW) super-conducting ion Linear accelerator (iLinac) with a high-energy synchrotron to produce various stable and radioactive intense beams with high energies. The ma-chine has a versatile operation mode which requires a high flexibility and reliability to the Machine Protection System (MPS). A customized and robust MPS is designed and developed to give the readiness of the machine for operation, to mitigate and analyze faults related to the relative damage potential. To get a high speed and have a high level of reliability, all interlock signal processing is processed on radiation-tolerant Field-Programmable Gate Arrays (FPGA) with triple or dual redundancy, as well as with a fail-safe design. By implementing a multiprocessing platform system-on-chip FPGA, the HIAF MPS can be tightly integrated with other systems to maximize availability pinpoint failures for operations, and give the postmortem analysis. This paper will describe the architecture of the interlocks linking the protection systems, the strategies to manage the complexity, the detailed components, and the interlock logic of the customized HIAF MPS, as well as the test and verification of the proto-type.

INTRODUCTION

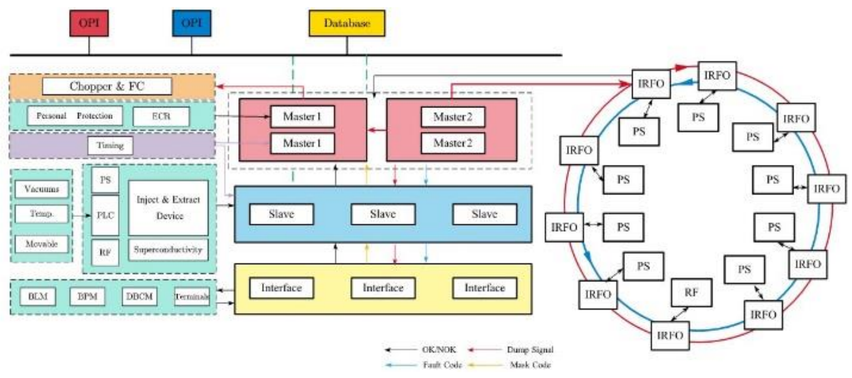
The High Intensity Heavy-ion Accelerator Facility (HIAF) is a next-generation research facility for heavy-ion science and technology that features unprecedented beam intensities and broad beam energies. HIAF consists of SECR (superconducting electron-cyclotron-resonance ion source)、iLinac(ion Linear Accelerator)、 BRing(Booster Ring)、HFRS(HIAF fragment separator)、 SRing(spectrometer ring) and several experimental terminals.





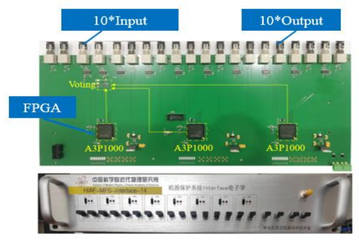
The whole machine is split into 13 sections and the logic of the MPS is to combine different sections to meet different operation modes. To have a high flexibility, the whole accelerator is partitioned by 2 master controllers master and 8 slave controllers slave.

HIAF MPS STRUCTURE



The masters, the slaves and the interfaces formed a three-layer tree structure. The master and the interlocking fan-outs（IRFO） form a daisy-chained ring structure. interface adopts a triple-redundant design, mainly accessing the interlocking signals from the beam diagnostic equipment BPM, BLM and BCM, and then connecting to the slave after logical determination. Salve also adopts a triple-redundant design, collecting the signal from the interface and the inter-locking signals from the power supply, radio frequency, injection extraction system and the PLC (Program-able Logic Controller) controller of the slow protection system. Master is a dual redundant design, collecting signals from the slave and the highest priority systems such as the ion source and the personal protection system.

HARDWARE & FIRMWARE

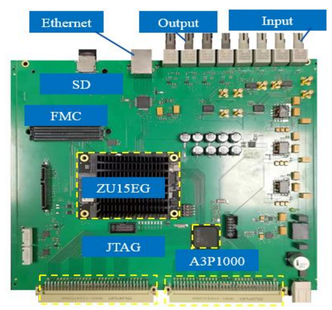


The hardware of the interface electronics is shown in Figure left top shown. To achieve high speed and get a high level of reliability and flexibility, all signal processing on the interface is accomplished with triple modular redundancy (TMR) technique, by using three FPGA chips working independently. In case the interface is located inside the tunnel and constantly in a radiation environment, the radiation-hardened A3P1000[4] from ProASIC3 Flash Family FPGAs is chosen because it is a flash-based device.

- Radiation-resistant FPGA: ProASIC3
- Triple module redundancy.
- Fibre-optic communication (10 MHz/20 MHz)

The interlocking fan-out electronics hardware as the figure left bottom shown. The main function is to fan out the interlocking signal to the power supply and radio frequency system in the Bring. It can feedback the working status of the power supply controller and self-test in the link. Ring interlock fan out are daisy-chained, using a clockwise and anti-clockwise double-loop circuit, using a modular design of the Manchester encoding method.

HARDWARE & FIRMWARE



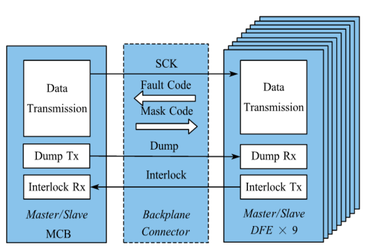
The Master/Slave electronics hardware as the figure left shown. The master and slave share a common hardware design. Master/slave controller is designed in a customised 6U chassis, the main part includes power supply, 9 digital front-end boards (DFE) and one main control board (MCB as the figure 6 shown). Adopting A3P1000 anti-radiation chip and ZU15 FPGA with ARM, each DFE can access 4 channels of user devices and supports optical fibre and Ethernet communication.

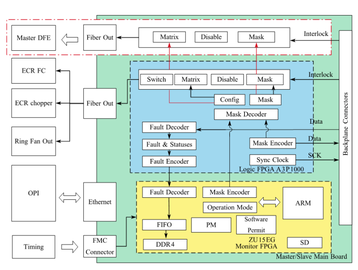
- Xilinx XCZU15EG
- ARM cortex-A53
- 16 GB SO-DIMM DDR4
- FMC connector for White Rabbit.

HARDWARE & FIRMWARE

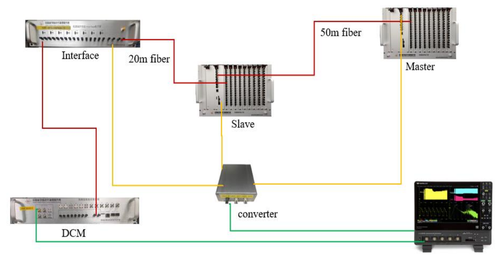
The master/slave electronics is mainly composed of MCB and DFE. 9 DFEs interact with MCB for interlocking signals and data at the same time through the high-speed plug-in backplane. A3P1000 is used as the logic chip on the DFE board, which is responsible for collecting the interlocking signals and fault information of the sub-devices, and sends them to the MCB board after decoding and encoding at the same time. There are two FPGA chips on the MCB, one is the radiation-resistant A3P1000 to perform the logic interlock function, and the other is the ZU15 with ARM to be responsible for the data interaction with the upper layer.

In the monitoring FPGA using ZYNQ IP core to complete the design of the system on chip, through the AXI4 bus to complete the PL side and PS side of the data transfer, can use the BRAM for interlocking information locking, integrated with the EPIC architecture to complete the release of the PV. Various soft signals, including soft interlock, timestamp, and interlock status data are done on the monitoring FPGA-ZU15。





The HIAF MPS prototype is built for performance demonstration as the figure 10, which include differential current monitor (DCM) electronics for the interlock input, interface electronics, a slave, and a master controller. The interface collects the user interlock signal from the DCM electronics. The MPS response time is about 4.6 μs for the whole system. The yellow wave is the interlock input from the DCM, and the green is a dump signal from the master controller.



CONCLUSION

The HIAF MPS system prototype is built and the function is verified, which meets the project requirements. The whole system is highly reliable with high speed in 4.6 μs from OK/NOK inputs to mitigation outputs。However, system integration into the HIAF complex and commission challenges lay ahead.