Development Of Bunch-by-bunch Beam Charge Monitor For High Energy Photon Source

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INTRODUCTION

- The High Energy Photon Source (HEPS), is the first fourth-generation synchrotron light source in China.
- HEPS consists of a 500 MeV LINAC, a booster synchrotron and a 6 GeV storage ring.
- Bunch Charge Measurement (BCM) system is built to help the commissioning of HEPS for the booster and ring respectively.

SYSTEM OVERVIEW

The BCM system consists of three main parts:

- The BPM pickup generates pulse signals with a repetition frequency of 499.8 MHz, and each pulse corresponds to one beam bunch.
- The front-end electronic imports the signals from the BPM, and then adjusts them. The signals are input to the signal processor and are converted to digital numbers using high-speed digital-to-analog converters (DACs).
- The software converts the ADC bits to charge, displays the BCM data in the right order of bunch number, and updates the corresponding EPICS variables.

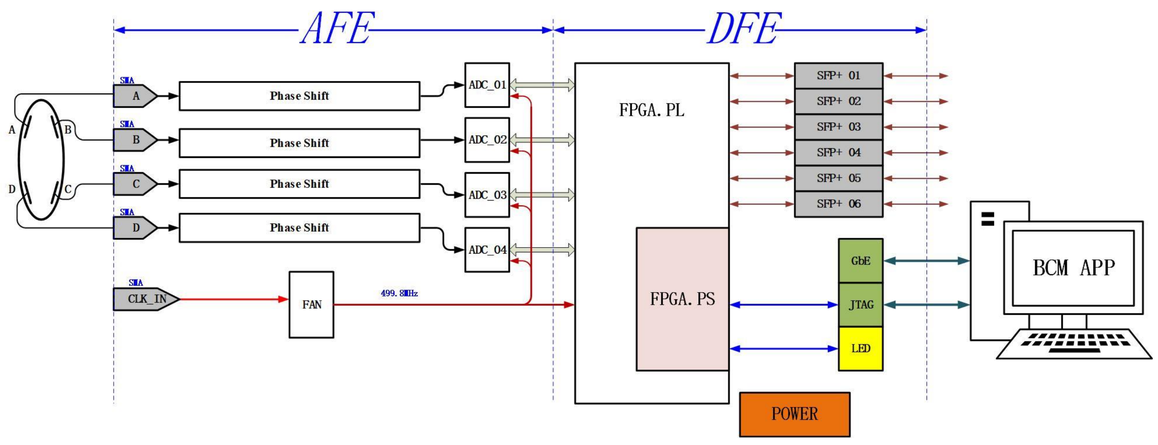

Figure 1: System diagram of BCM.

HARDWARE. AFE

The AFE, which consists of four modules, is used to digitize the bunch-by-bunch signal at frequency of 499.8 MHz.

- High speed sampling module. In this module, the signal passes through two stages of balun, the ADC chip, and the driver chip in sequence. The ADC has a sampling rate of 499.8MHz, a significant number of 12 bits, and a bandwidth of 1GHz.
- High-speed clock fan out module. This module can output 5 low-jitter clocks. Four of them are provided to the ADCs as sampling clock and one of them is provided to the DFE as master working clock.
- Delay Adjustment module. ADCs should sample at approximately the peak of the signal and the sampling clock should be precisely adjust the time delay. The delay adjustment circuits can meet this demand.
- Low noise power supply module. This module contains a two-stage power supply circuit that provides a noise RMS value of less than 40μV for the analog signal acquisition board to meet the needs of high-precision sampling for bunch-by-bunch electronic systems.

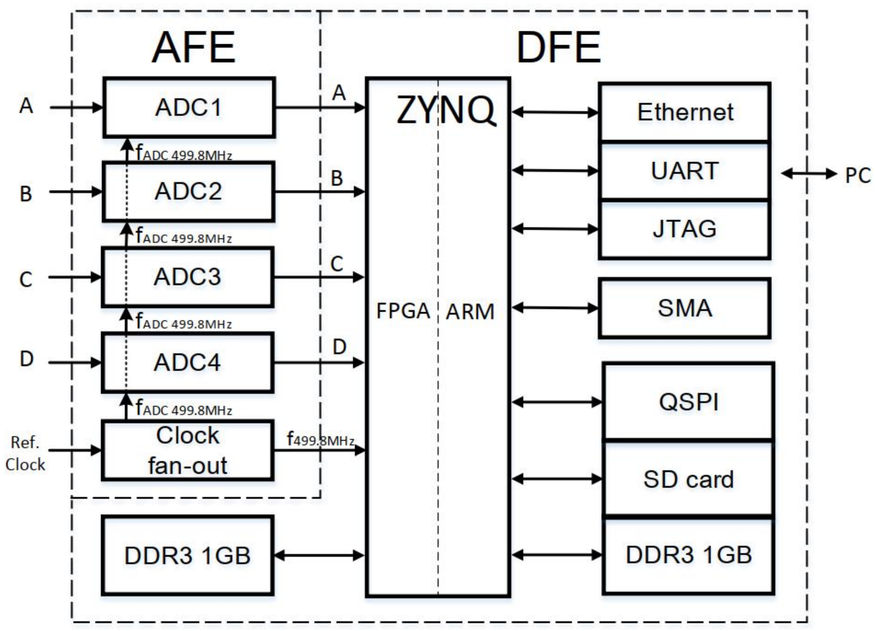

Figure 2: Hardware diagram of BCM.

HARDWARE. DFE

The main circuit of the DFE is a field-programmable gate array (FPGA) .

- The main module of the DFE is ZYNQ-7000, which consists of two hard processors (PS), programmable logic (PL), and many other features all in one silicon chip. The PL part is used to process the bunch data from ADCs and the PS part is used to run embedded Linux and the EPICS application software.
- The DFE board contains 2GByte DDR. In addition to the space occupied by the operating system, there is 1.5GByte space to store data.
- The communication module consists of JTAG interface, serial port and Ethernet interface.

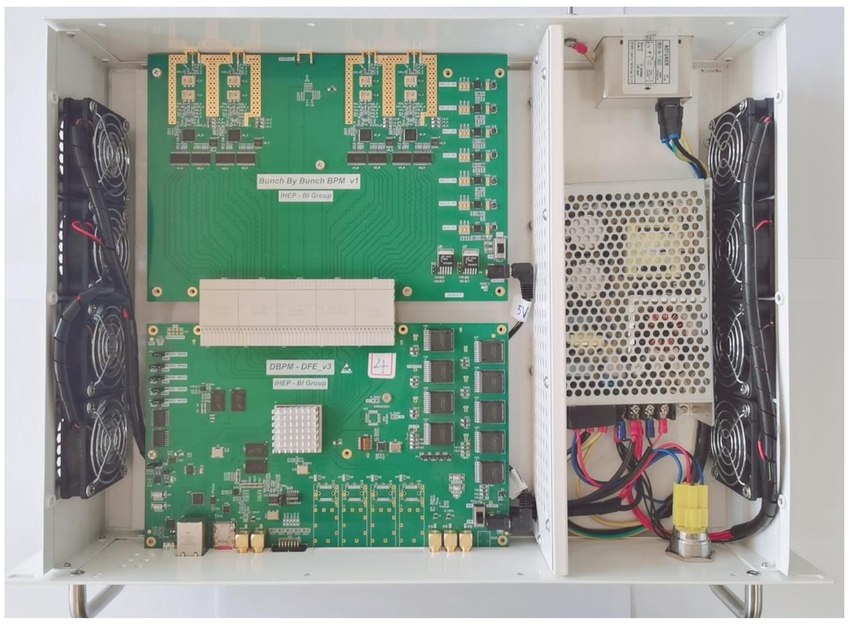

Figure 3: Picture of real BCM electronic products.

SOFTWARE

- Being developed based on EPICS, the BCM software is well integrated into the overall HEPS control system.
- Setting up of the desired delay time. The first stage is coarse time adjustment with a step size of 150 ps; the second stage is fine time adjustment, a precise adjustment with a step size of 1 ps.
- Calculating the absolute bunch charge. The bunch charge is determined by the proportion of each bunch charge in all bunches and the average current value measured by the direct-current current transformer (DCCT) system.
- Sending the bunch charge data to the control net-working. The data being shown is transmitted to client software from the BCM hardware through the TCP/IP connection.

INITIAL USE IN HEPS

- There are two BCM systems built on the HEPS, one for the HEPS booster and the other for storage ring.
- The bunch charge in each bucket can be monitored in the Central Control Room. As shown in Figure 4 and Figure 5, the operators can monitor the bunch charge and the number of bunches.

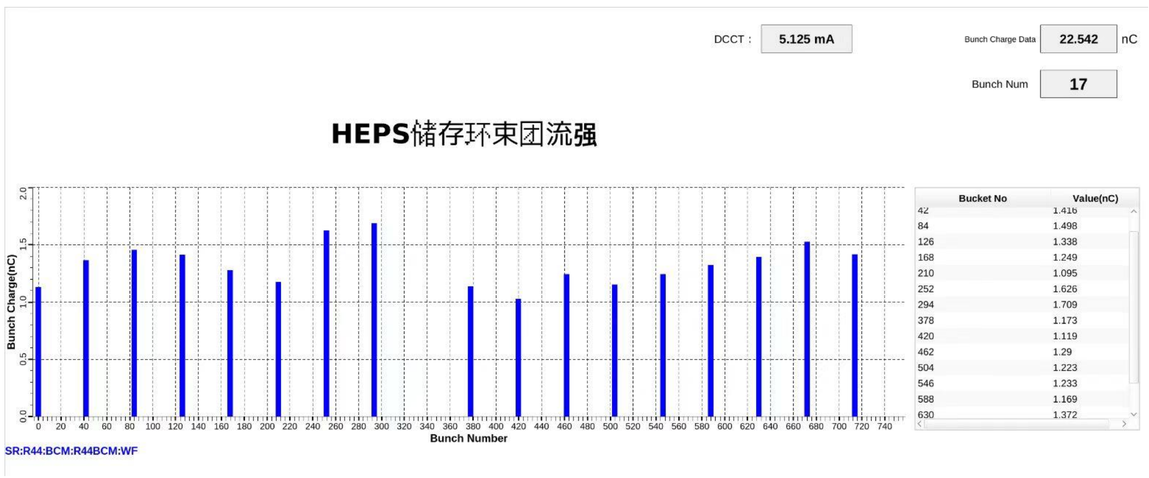

Figure 4: Display of BCM system (storage ring) in HEPS commissioning.

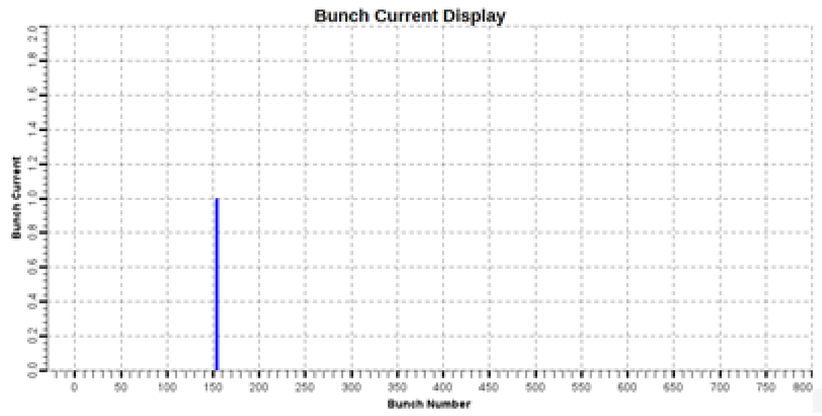

Figure 5: Display of BCM system (booster) in HEPS commissioning.