High-resolution quad channel picoammeter: characterization and commissioning

Lucas Tanio*, Fernando Cardoso, Mauricio Donatti
Brazilian Synchrotron Light Laboratory (LNLS)

Hardware design

Simplified Block Diagram

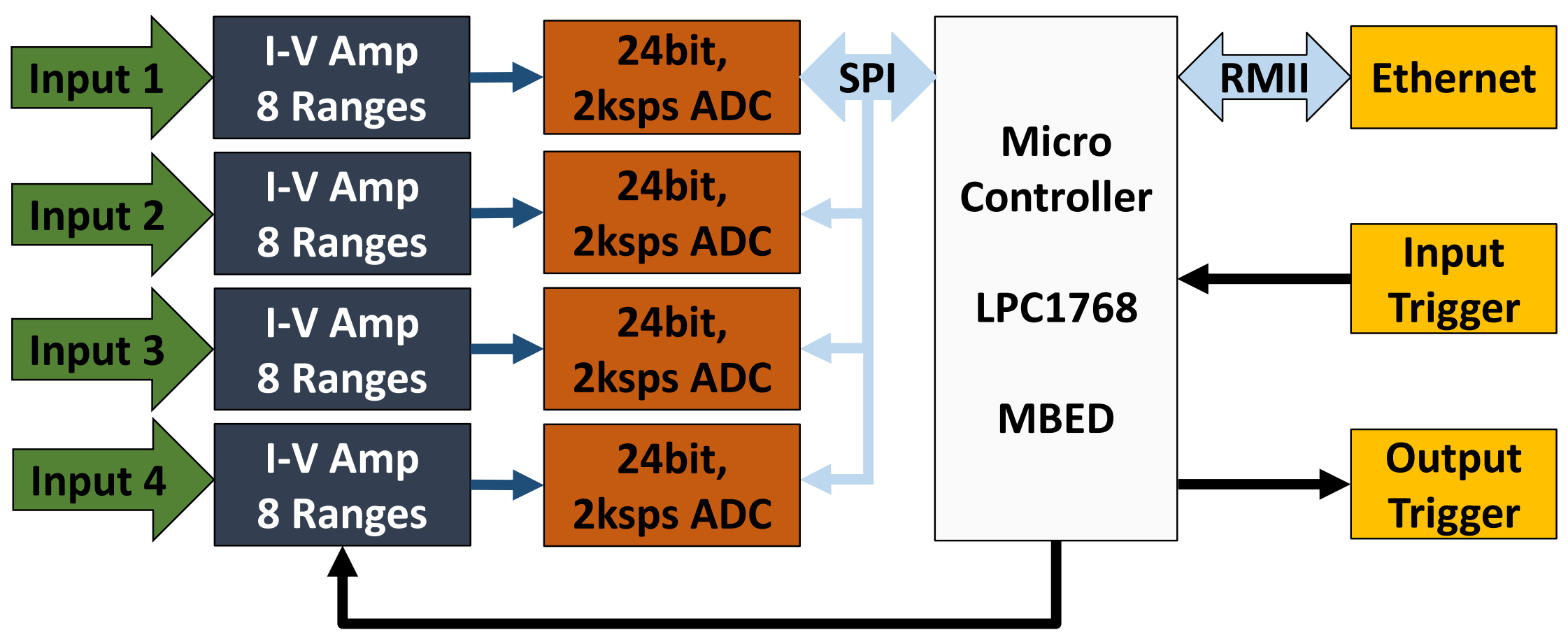


Fig 1. *Quad channel picoammeter - simplified block diagram*

- Current to voltage amplifier
  - ✓ Transimpedance topology
  - ✓ 8 selectable ranges
- Analog to digital converter
  - ✓ Σ-Δ topology
  - ✓ 24-bit resolution
  - ✓ 10 selectable sampling rates
- Microcontroller
  - ✓ 32-bit
  - ✓ ARM Cortex-M3
- Trigger interface:
  - ✓ Input voltage trigger range (3.3 V to 27 V)
  - ✓ Output trigger capable of driving 50Ω load at 5V.

Analog front-end bandwidth analysis

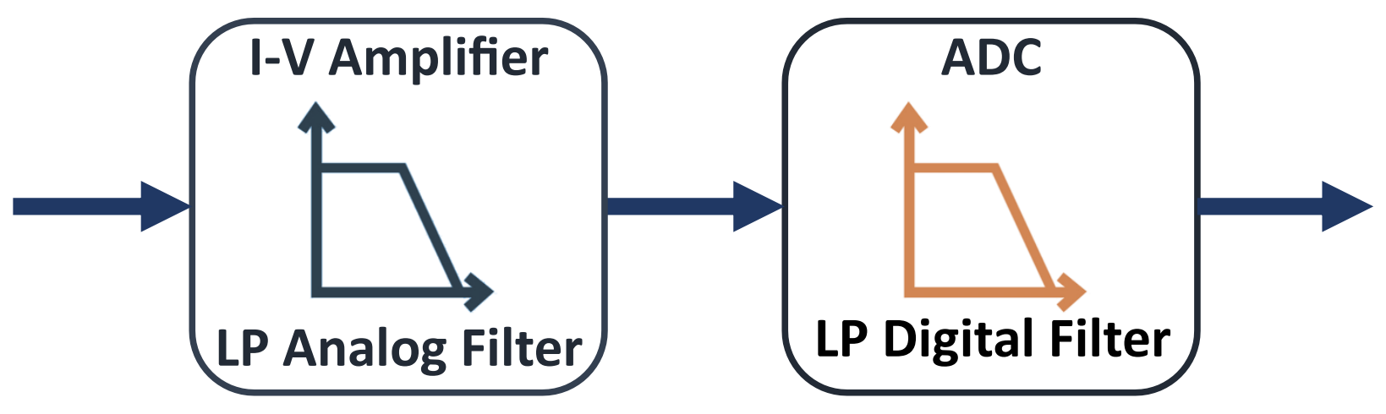


Fig 2. *Analog front-end block diagram*

How can I fully characterize the quad channel picoammenter bandwidth?

Problem:

- Number of combinations: 8 scales x 10 sampling rates
- The sine sweep procedure is time costly

Solution:

- Perform the sine sweep procedure for 2000 SPS;
- Use a numerical fitting algorithm to find the front-end filter parameters;
- Estimate the bandwidth using filter parameters and ADC datasheet

Table 1. *I-V amplifier main characteristics*

Scale	Full Scale	Sensitivity	Analog Bandwidth
1	250 pA	100 pA/V	16 Hz
2	2.5 nA	1 nA/V	154 Hz
3	25 nA	10 nA/V	702 Hz
4	250 nA	100 nA/V	702 Hz
5	2.5 µA	1 µA/V	702 Hz
6	25 µA	10 µA/V	702 Hz
7	250 µA	100 µA/V	702 Hz
8	2.5 mA	1 mA/V	702 Hz

Table 2. *ADC sampling characteristics*

Sampling Rate (SPS)	Digital Filter Bandwidth (Hz)	Oversampling Ratio
5	2	6400
10	5	3200
20	15	1600
40	9	3200
80	20	1600
160	118	800
320	154	800
640	495	400
1000	732	256
2000	1465	256

Triggered mode: time analysis

Time analysis setup:

- Four channels enable
- ADC sampling rate equals to 2000 SPS
- Number of samples per trigger pulse equals to one

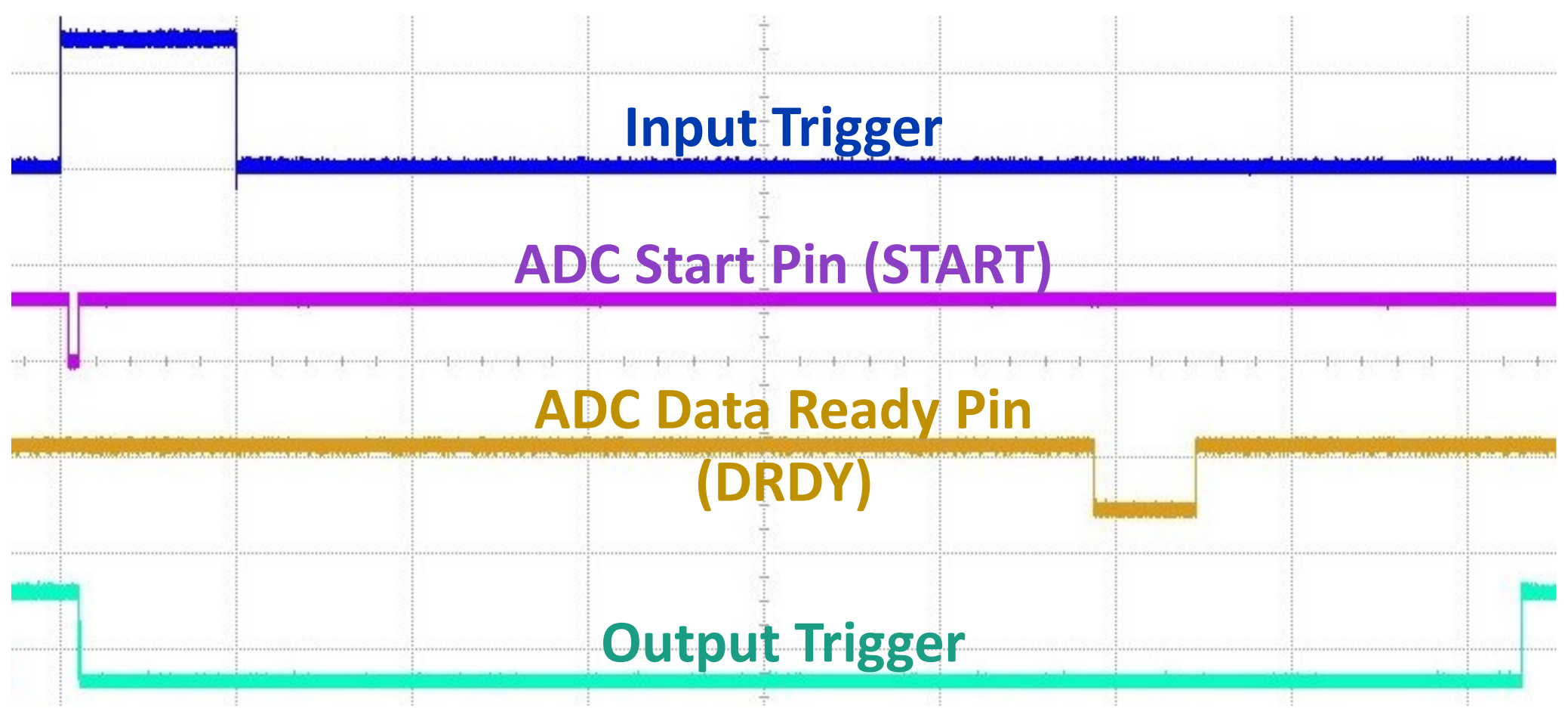
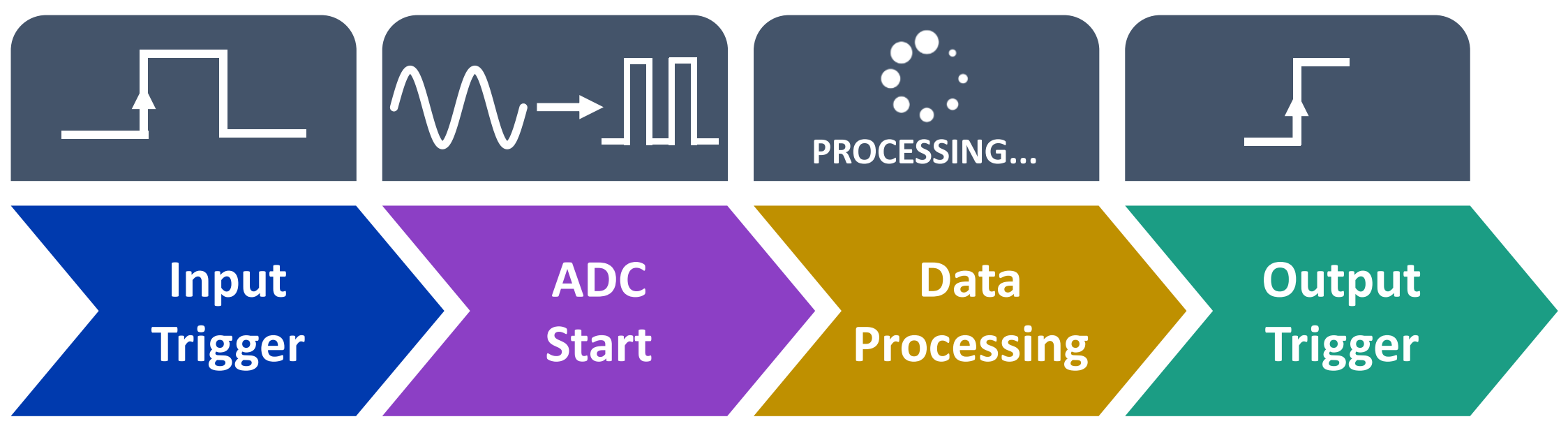


Fig 3. *Time diagram in trigger acquisition mode*



Input Trigger

1.The device receives a rise edge trigger

2.The **Output Trigger** and the **START** are switched to low-state

ADC Start

3.The **START** is shifted to high-state and the ADC begins the conversion

Data Processing

4.When the **DRDY** changes to low-state, the conversion is over and the µC starts the data processing

Output Trigger

5.The **DRDY** state shifts and the data is sent over the Ethernet connection

6.The **Output Trigger** is switched to a high state

How long does it takes to acquire one sample?

$$t_{tot} = t_{scd} + t_{ADC} + t_{\mu C} + t_{eth} \quad (1)$$

What is the maximum trigger frequency?

$$f_{trg}^{max} = \frac{1}{t_{tot}} \quad (2)$$

Table 3. *Timetable description in triggered acquisition*

Name	Symbol	Description
Start Conversion Delay	t_{scd}	The time interval between rising edge input trigger and rising edge START
ADC Conversion Time	t_{ADC}	The time interval between rising edge START and falling edge DRDY
Microcontroller Processing Time	$t_{\mu C}$	The time interval between DRDY falling edge and rising edge
Ethernet Circular Buffer Transfer Time	t_{eth}	The time interval between DRDY rising edge and output trigger rising edge
Total Time	t_{tot}	The time interval between rising edge input trigger and rising edge output trigger

Results

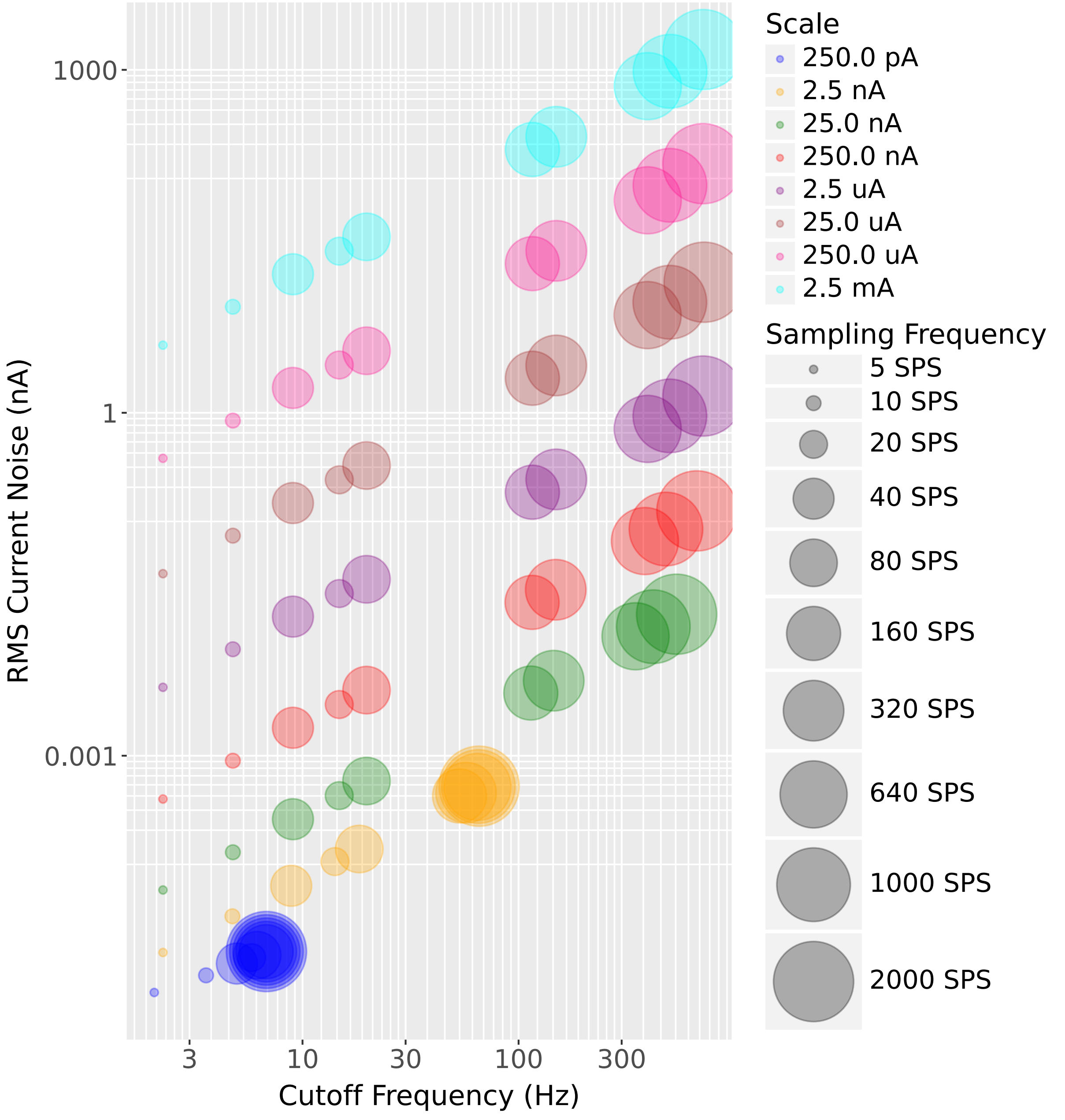


Fig 4. RMS noise current vs. cutoff frequency for each scale and sampling rate

The linear fitting was successfully validated as the maximum frequency coefficient variation (ratio between the mean value and the standard deviation) ranges from 7% to 10% (low variability).

Then, the RMS current noise can also be determined using Eq. (3), where bandwidth values are obtained by the curve fit and the noise spectrum density at 2000 SPS discussed in previous works [1]. The average value of cutoff frequency and RMS noise current for each scale and sampling rate are summarized in Figure 4.

$$i_n^{RMS} = \sqrt{\int_{f_{min}}^{f_c} \left(i_{n_{den}}^{RMS}\right)^2 df} \quad (3)$$

Table 4 summarizes the trigger mode time analysis where there are the values of the conversion time, the maximum trigger frequency, and signal bandwidth. Eq.(2) has been used to estimate the maximum trigger frequency, considering the employed time was the total time mean value added to the standard deviation multiplied by 3. The signal bandwidth was calculated using Eq.(4).

$$BW_{sig} = \frac{F_{TrgMax}}{2} \quad (4)$$

Table 4. *Estimated conversion time, maximum trigger frequency, and maximum signal bandwidth for each ADC sampling frequency*

Sampling Rate (SPS)	Conversion Time (ms)	Maximum Trigger Frequency (Hz)	Signal Bandwidth (Hz)
5	200.6	4.9	2.5
10	100.9	9.9	5.0
20	51.1	19.5	9.8
40	25.5	39.1	19.6
80	13.0	76.5	38.3
160	6.8	146.1	73.1
320	3.6	277.4	138.7
640	2.0	487.9	244.0
1000	1.4	668.6	334.3
2000	0.881	1070.0	535.0

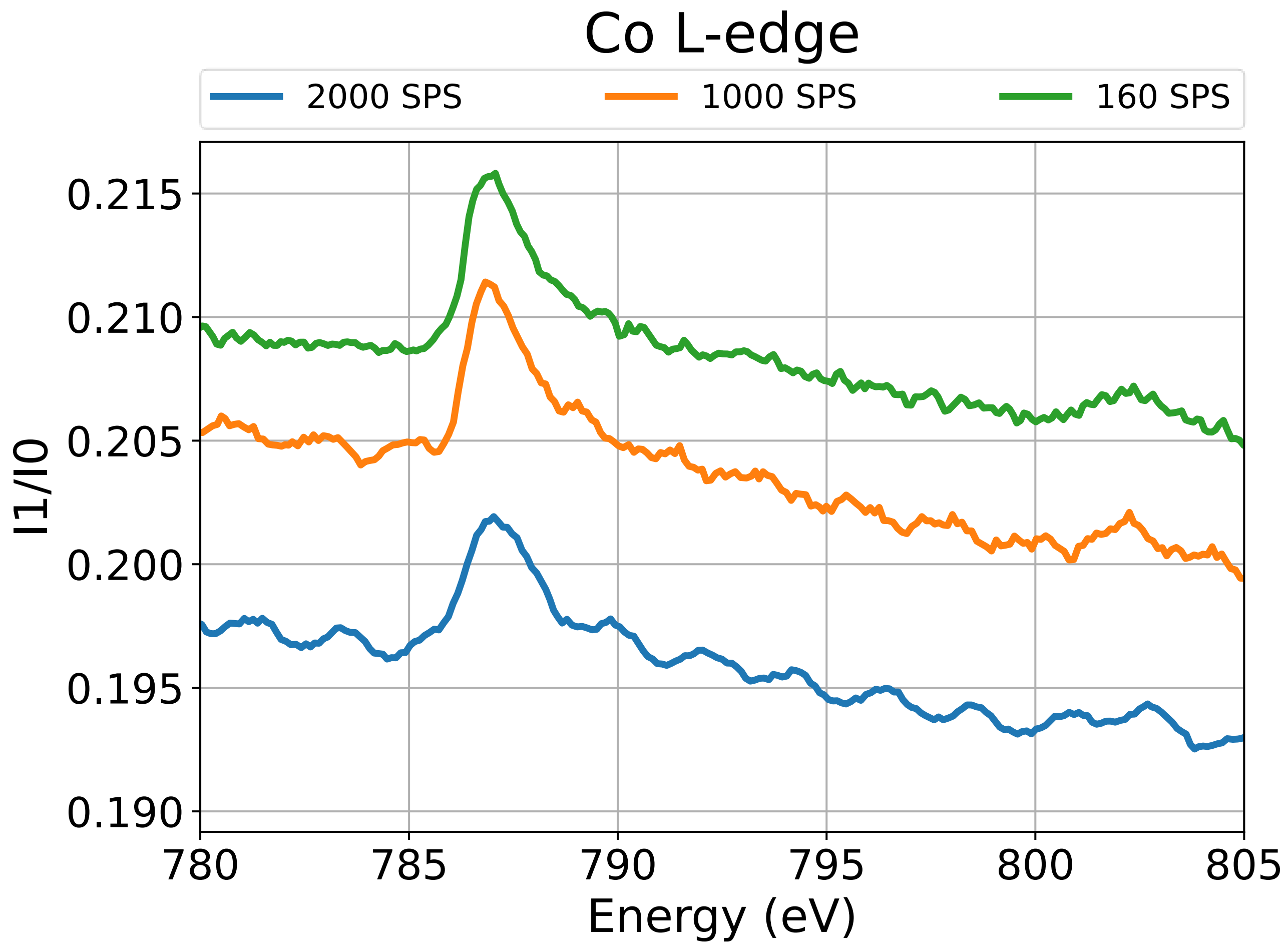


Figure 5 shows a practical problem found in a beamline experiment where the electron mobility of a specific material is low, and the measured current is noisy. An alternative to mitigate this problem is to change the ADC sampling rate to find a better signal-to-ratio response.

Fig 5. . Cobalt (Co) L-edge Absorption Spectrum for different ADC sampling frequencies

Conclusion

The linear fit algorithm that describes the frequency response for each combination of transimpedance scale and the ADC sampling frequency was homologated by the statistical analysis as well as the RMS current noise.

From the time analysis at triggered mode, it was possible to estimate the amount of time for acquire one sample, and consequently assess the maximum trigger frequency and the signal bandwidth.

Finally, the measurements at Sabia beamline, using the on-the-fly scan technique, validates the reliability and repeatability of the quad channel picoammeter.

Acknowledgments

The authors would like to gratefully acknowledge the funding by the Brazilian Ministry of Science, Technology and Innovation (MCTI), and the contributions of the LNLS teams enrolled in Sirius project.

References

[1] M. M. Donatti, F. H. Cardoso, L. Y. Tanio, Development of a quad-channel high-resolution digital picoammeter for beam diagnostics. 2024 JINST 19 C03028. [DOI:10.1088/1748-0221/19/03/C03028]

*lucas.tanio@lnls.br