A high-precision low-latency DBPM processor for HALF

Jiajun Qin, Yi Tang, Kexi Hou, Zhenyan Li, and Lei Zhao

State Key Laboratory of Particle Detection and Electronics,

University of Science and Technology of China, Hefei, Anhui, P. R. China

1. Introduction

Hefei Advanced Light Facility (HALF) is a fourth-generation vacuum ultraviolet and X-ray diffraction limit synchrotron radiation (DLSR) light source under construction. It is expected to have an ultra-low emittance and an extremely small beam size, which requires high-precision orbit detection and fast feedback control. The processor is the key component of the digital beam position monitor (DBPM) and control system, which is required to provide a position resolution of less than 200 nm in Fast Acquisition (FA) mode at a sampling rate of approximately 20 kS/s with a processing latency of lower than 90 μs. This paper presents the design of a HALF Digital Beam Position Monitor (DBPM) prototype electronics. To achieve the desired high position resolution and low latency, we analyze the key factors influencing position resolution and system latency within the beam position monitor system. The design incorporates a pilot tone compensation structure, low-noise analog manipulation, and a low-jitter sampling clock to enhance resolution. Furthermore, a higher sampling frequency combined with a low-order digital low-pass filter is employed to minimize latency.

2. Circuit Design

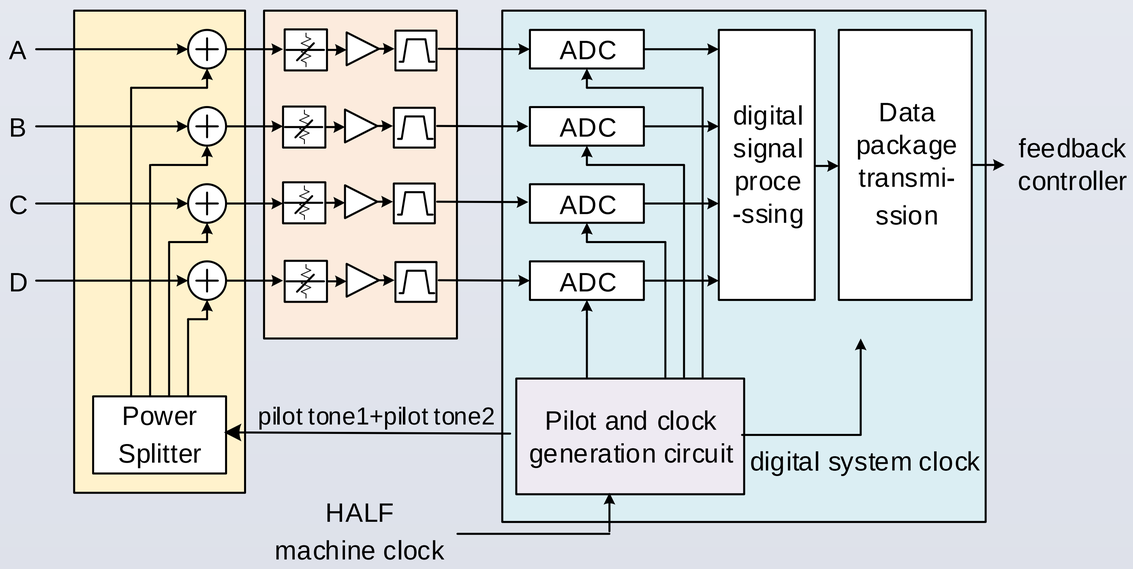
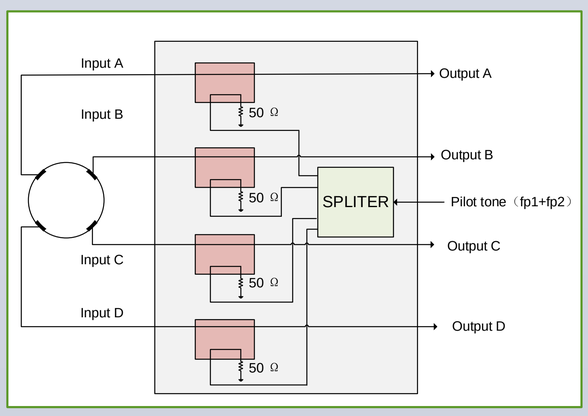


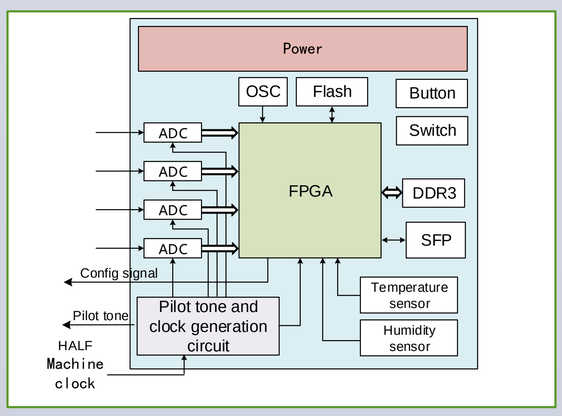
Fig. 1. Block diagram of the DBPM processor prototype.

Fig.1 shows the block diagram of the DBPM electronics prototype. The system is composed of three main modules: the pilot tone coupling module, the analog manipulation module, and the digitization and digital signal processing module. Within the pilot tone coupling circuit, the four input signals are coupled with dual pilot tones. After coupling, the signals undergo amplification and filtering before being digitized. The digital signal processing stage then separately extracts the amplitudes of the beam signal and pilot tones. The beam position is subsequently calculated, using the pilot tone amplitude for calibration. In this system, both the sampling clock and pilot tone are generated by phase-locked loops (PLL), with the HALF machine clock serving as the clock source.

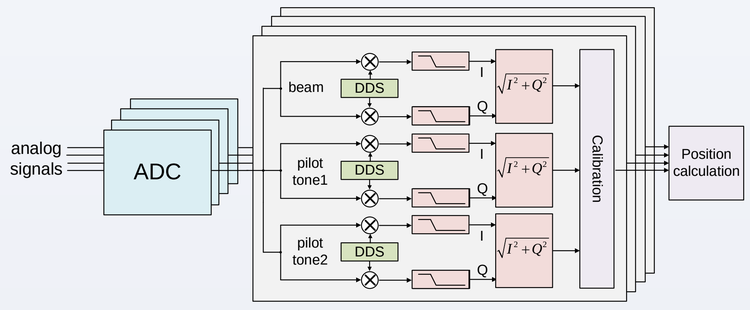
Fig.2 depicts some block diagrams of key components and FPGA logic of the prototype electronics.



(a) Block diagram of the pilot tone coupling module.



(b) Block diagram of the digitization and digital signal processing module.



(c) Block diagram of the FPGA logic.

Fig. 2. Block diagrams of some key components.

3. Performance

Fig. 3. Test setup.

Fig.3 shows the DBPM electronics prototype under test. In HALF, the input power of signal to the front end of the BPM processor is expected to range from -69.5 dBm to -17.4 dBm, corresponding to a beam current of 1 mA to 400 mA. For an input power of -17.4 dBm corresponding to a beam current of 400 mA, the resolution was measured to be 87.3 nm(horizontal)/88.1 nm(vertical) in FA mode at an update rate of around 20 kHz, 365.6 nm(horizontal)/386.8 nm(vertical) in TBT mode at an update rate of 624.75 kHz, 18.8 nm(horizontal)/17.0 nm(vertical) in SA mode at an update rate of around 10 Hz. The value of Kx,y in the calculation is 9.2 mm. Fig.4 shows the horizontal and vertical position in 10 seconds in FA mode

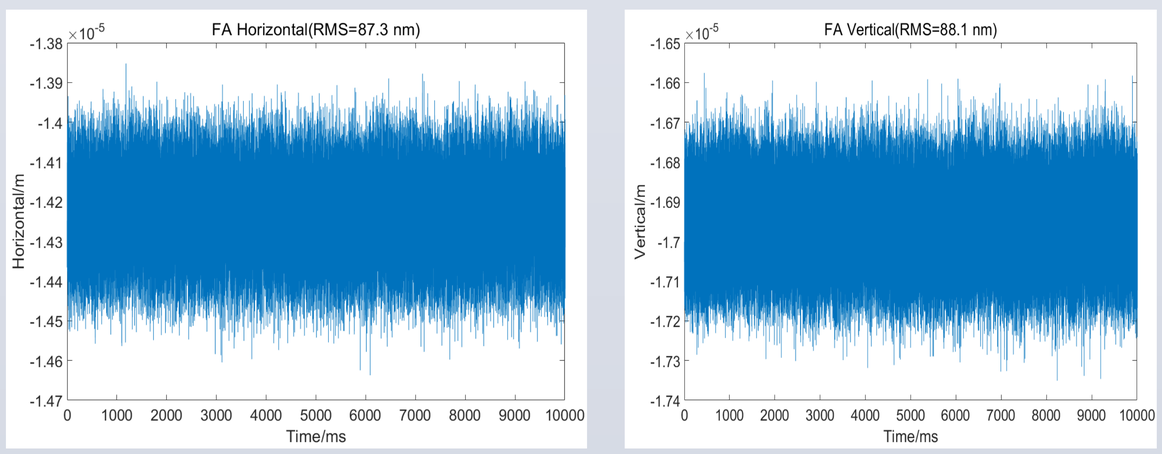
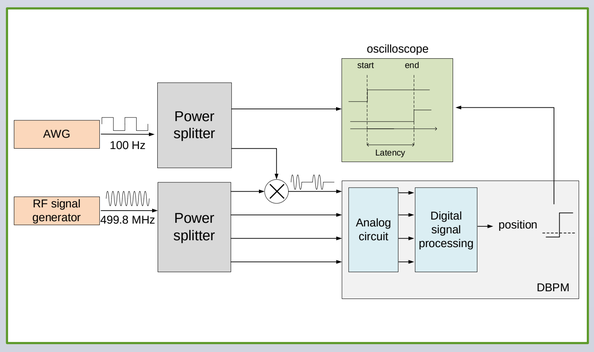


Fig. 4. Horizontal and vertical FA position data.



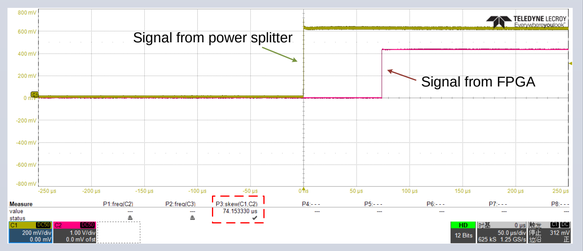


Fig. 5. Latency test.

The block diagram of the latency test setup is depicted in Fig.5, and the test result shows that a latency of less than 80 μs is achieved.