

散裂中子源 **China Spallation Neutron Source**

PRELIMINARY RESEARCH AND DEVELOPMENT OF BPM ELEC-**TRONICS UPGRADE FOR THE RCS RING IN CSNS II**

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I. Introduction

With the initiation of the Phase II project of the China Spallation Neutron Source (CSNS II), the target power is anticipated to increase significantly to 500 kW in the future. Upgrading the existing 32 sets of BPM electronics on the Rapid Cycling Synchrotron (RCS) ring is necessary to accommodate the increased beam power and meet the new requirements of the bean measurement.



V. System Testing

- □ The zero-input noise of the electronics with the detector, in the absence of beam current, was found to be below 3mV. □ The electronics have good linearity and INL..
- **D** ENOB was determined to exceed 9.5





Distribution diagram of beam measurement components in CSNS.

II. ELECTRONICS SYSTEM

In the Rapid Cycling Synchrotron (RCS) of the China Spallation Neutron Source (CSNS), there are four quad-rants, each equipped with 8 BPM detectors. The dual-bunch revolution frequency ranges from 1 MHz to 2.44 MHz, with the bunch length compressed from 500 ns to 100 ns. Each bunch completes approximately 20,000 turns within an acceleration cycle of 20 ms. The signal dynamic range of the BPM is 10^4.

> LPF Sampling Granularity Facility MHz bit rate

VII. Beam-On Experiment

During the operational phase of the accelerator, exper-iments were performed utilizing the RF BPM in RCS. The electronics were employed to capture and store the 20ms BPM signals for subsequent offline analysis. Furthermore, Libera electronics were utilized to store both the 20ms data and Turn-By-Turn (TBT) data from the RF BPM for comparative analysis with the CSNS electronics.



	MHz		
Libera Hadron	250	16	55
HIAF	250	16	20/300
J-PARC	40	14	5
CSNS	250	14	25

The electronics system is divided into two parts. The Front-End Controller (FEC) readout boards handle digit-izing the front-end signals, conducting real-time beam position calculations, and buffering raw ADC data and position data. The System-On-Chip (SOC) data aggrega-tion boards manage reading data from 8 FECs, with a front-end data bandwidth of 80 Gbps. They package the data, distribute it to the server, and configure the FECs. Each local station in a quadrant consists of 8 FEC boards and 1 SOC board.

CSNS electronics ADC_RAW data was processed using a dual-threshold window algorithm

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