PROTOTYPE OF BPM ELECTRONICS FOR FEL-HMF

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Abstract

This paper presents a prototype of BPM electronics for experimental installation of free electron laser and high magnetic field (FEL-HMF). FEL-HMF integrates mid-long Infrared free electron laser, high magnetic field and cryogenic, which is a critical apparatus for new advanced materials especially for low power-consume electronic materials. The BPM electronics consists of two ADC chips and one FPGA SoC. The ADC has two channels, and sampling rate is 240Msps. The FPGA SoC implements high speed digital signal and data process. The logic part of FPGA SoC is running signal process. The processor part of FPGA SoC runs Linux operating system and EPICS-based user application program. This BPM electrons has been tested and analyzed in lab. Its X and Y position is ~1.4um (RMS).

INTRODUCTION

The experimental facility of free electron laser and high magnetic field (FEL-HMF) is been building by Anhui University in Hefei, China. It is the first large-scale scientific facility constructed by Anhui university and is a unique integration of free-electron laser, high magnetic field, and low-temperature environment. This cutting-edge technology is a vital tool for studying the energy level structure of materials, dynamical processes, and other scientific issues. The facility is primarily concerned with the investigation of quantum materials, with a particular emphasis on low-power electronic materials. However, it also serves as a crucial experimental platform for a diverse range of multidisciplinary frontiers, including energy materials, biomaterials, medicine, and health materials. It includes five experimental stations：

- The Ultrafast Infrared Spectroscopy Experimental Station
- The Scanning Probe Microscopy Station
- The Magneto-Optical Experimental Station
- The Multi-field Control Experimental Station
- The Integrated Characterization Station

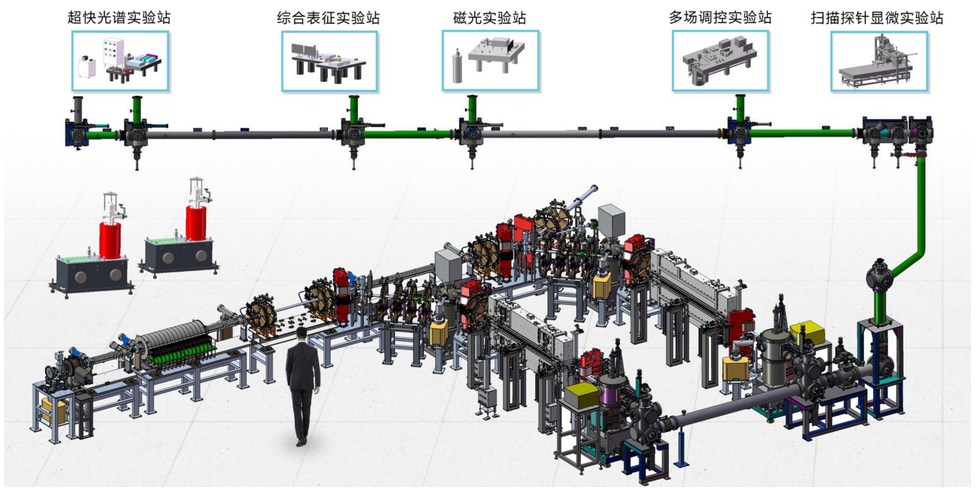

Figure 1 Model of FEL-HMF

BEAM POSITION MONITOR ELECTRONICS

RF Front-end

The RF front-end gain control circuit employs two cascades to achieve 40dB amplification of the RF signal, and a one-stage adjustable attenuator to achieve a 31.5dB gain adjustment range.

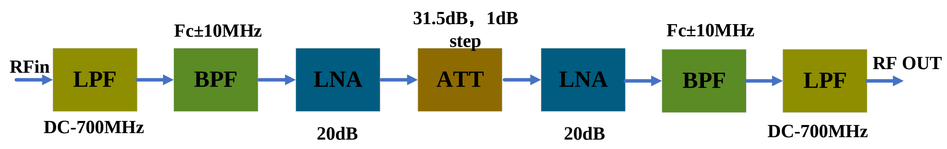

Figure 2 overview of RFFE chain

Signal Sampling

The RF front-end output is converted to differential signals via the ADC front-end matching circuit and subsequently sent to the ADC chip for sub-sampling. This output data is then sent to the FPGA for processing.

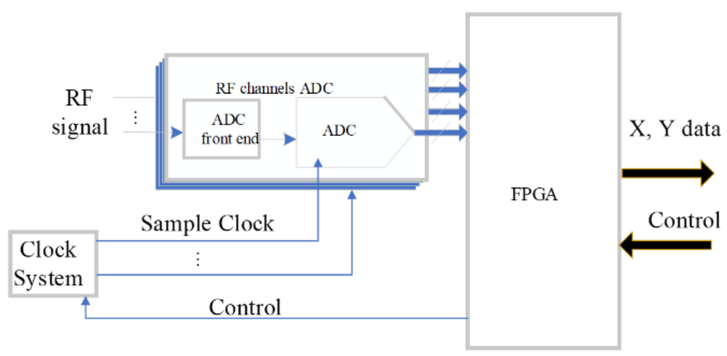

Figure 3 Diagram of Signal sampling

Logic Design

The FPGA logic employs two distinct magnitude calculation algorithms: time-domain magnitude calculation and DDC-based magnitude calculation. The process of time-domain amplitude calculation is to take the square of the ADC raw data and then run square root. The DDC-based amplitude calculation process employs the DDC to facilitate digital I/Q de-modulation, thereby obtaining I and Q. The I/Q sequences are transmitted to the DMA module for subsequent transfer to the ARM processor in the SoC, following the application of low-pass filtering and extraction operations. Data processing is then conducted within the ARM processor.

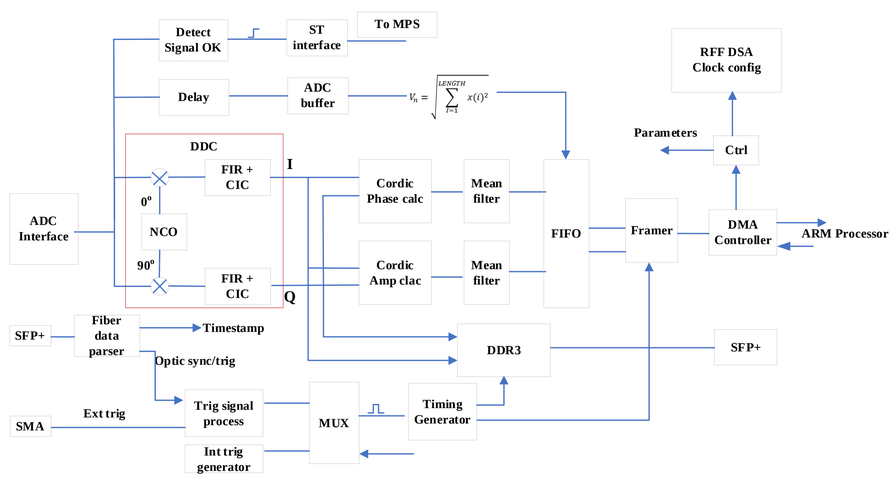

Figure 4 Flow diagram of FPGA logic design including digital signal process and control

Software Design

A Linux operating system was running on the ARM-based system-on-chip (SoC), and an application was developed for that system. The principal functions of the program are as follows: The system incorporates a variety of advanced functionalities, including direct memory access (DMA) fetch, IQ amplitude and phase compensation, calculation of position X, Y and SUM, an EPICS server, and comprehensive control over RF gain, clock configuration, ADC dynamics, sample depth, and other parameters.

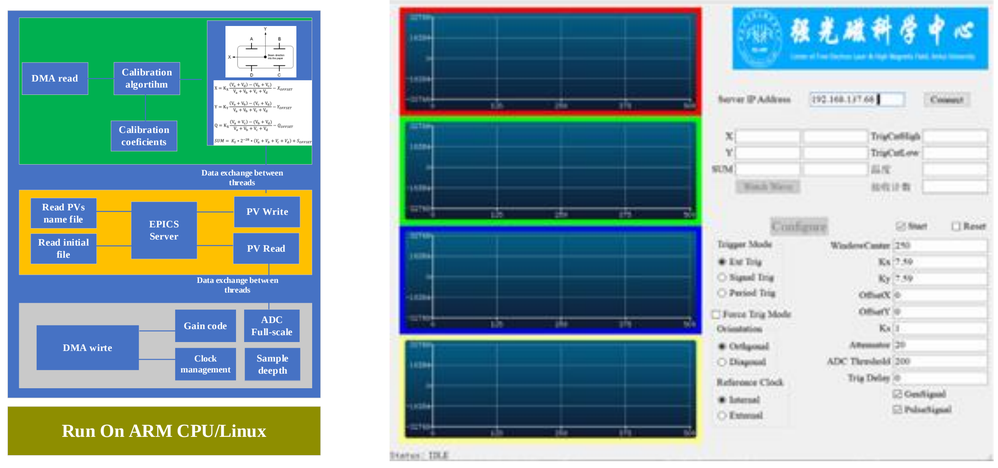

Figure 5 BPM software

Lab Test

A signal generator is employed to generate the test signal, which is transmitted to the electronics via a 1:4 power divider. Figure 8 illustrates the results of ~1300 pulses, x and y, with a mean value of 0.09mm and a standard deviation of 0.0014mm for x and a mean value of -0.25mm with a standard deviation of 0.0014mm for y. These values were obtained using the time-domain processing method and assuming kx = ky = 10 mm.

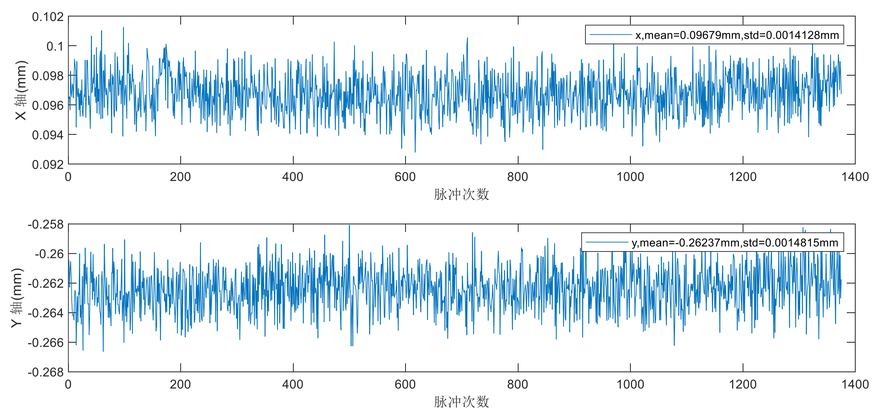

Figure 6 X and Y values of ~1300 pulses

CONCLUSION

The prototype of BPM electronics has been developed for FEL-HMF, which consists of one RF front-end processing module and signal acquisition and processing module. The RF front-end processing module enables filtering of spurious signals and conditioning of signal amplitude. Signal acquisition and processing module adopts ADC for sampling and uses FPGA SoC for high-speed signal processing and data processing. The logic part of FPGA SoC is running signal process. The processor part of FPGA SoC runs Linux operating system and EPICS-based user application program. This prototype of BPM electrons has been tested in lab and its performance meets the requirements.