

Design of Beam Position Monitoring Interlocking Projection Svstem



The machine protection system guarantees the safe operation of the HIAF in different operating modes and prevents damage to the online equipment in the event of a failure. Beam current data such as beam current position and phase is an important basis for analyzing and diagnosing accelerator faults. In this paper, the beam position and phase interlock monitoring system were designed by the authors. The system is based on circular buffer and AXI4 protocol to realize the transmission and storing of interlock data and locking of interlock status. Laboratory tests show that the system could save the beam position, beam phase, SUM signals and amplitude of sensed signal with interlocking before and after 8ms and latch the interlock status of 25 channels. The system was deployed at the CAFe-LINAC (LINear ACcelerator) in March 2024 and completed online measurements.

The [1-2]is a new-generation heavy-ion accelerator research device with international leading level. It could provide the highest peak flow of low-energy heavy-ion beams in the world. In order to avoid radiation damage to on-line equipment in the event of a malfunction and to increase the availability of the entire installation. The Beam Position and Phase Interlock Protection System monitors physical quantities such as the horizontal position of the beam, the vertical position, the SUM signal the beam intensity and the beam width of the pulsed beam. The system would send an interlocking signal to the [3] before a fault occurs or in the shortest possible time after a fault occurs. Simultaneously, the beam data would be saved in the local computer. The system provides a reference for beam commissioning, machine studies and beam structure analysis.



Figure 1 block diagram of the system

Table 1: Monitored state quantities			
State Quantity	state	note	
ADC raw value	saturation	4 channels	
beam intensity	high	H1 & H2	
beam intensity	low	H1 & H2	
phase	high	H1 & H2	
phase	low	H1 & H2	
horizontal position	high	H1 & H2	
horizontal position	low	H1 & H2	
vertical position	high	H1 & H2	
vertical position	low	H1 & H2	
and a second	and appropriate the second		

In the system, the interlocking status of the monitored state quantities is latched and transmitted to the ARM (Advanced RISC Machine) and then published to the user interface through the network. In addition to the locking of state quantities, the beam data before and after the occurrence of the interlock is also very important. The beam data could be analyzed to determine why failures occur and could also

be used to predict failures. The authors used BRAM (Block Random Access Memory) as a buffer to store beam data in real time, including beam position, beam current intensity, beam phase and the sensed amplitude and phase of the four probes of the detector. The BRAM of the Zynq UltraScale+ MPSoC XCZU9EG is only 40.9 Mb, so the system could only store 8.192 ms of beam data at this stage. Since all the interlocking states are semaphores, the lightweight on-chip protocol



transmission effi-	high	H1 & H2
ciency		
transmission effi-	low	H1 & H2
ciency		

AXI-Lite is used in this system to transmit them to the ARM side. Data such as beam position, beam phase and beam intensity before and after interlocking are very important, especially for the analysis of faults and early warning of faults.

Figure 5: Flowchart of the reading state of a cyclic buffer



Figure 3: Test results with accumulators.

Interlock PARA Set Interface

trigger mode

PRAM_BEAM_EN_LEVEL 200

Figure 4: Reference signal waveform after trigger mode chaining.

overthreshold time

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The circular buffer works as follows: (1) The loop buffer is always in the write state when no interlock occurs; (2) The address is locked and sent to the ARM side when the interlock occurs; (3) The write state continues until the write pointer is offset 4096 from the locked address; (4) The ARM side starts reading data and the read pointer should be at the point where the lock address is offset 4096 forward; (5) Clear the interlock flag and enter the cyclic write state again. The flowcharts for the write and read states of the cyclic buffer are shown in Figure 5. That is equivalent to an interrupt program throughout the BPM's embedded system. When an interlock (interrupt) occurs, the system enters the interrupt handling program. The system would start to save beam data.

Conclusion: In this paper, the authors introduce a present a



SSBPM

Raw Data SPH Data Channel Amplitude Channel Phase

Figure 7: Waveform curve of the SUM signal of the monitored quantity SS-BPM

Figure 6: Online testing interface

Reference:

1. [J.C. Yang, J.W. Xia, G.Q. Xiao, et al., High Intensity heavy ion Accelerator Facility (HIAF) in China[J]. Nuclear Instruments and Methods in Physics Research B, 2013, 317(2013):263-265. Doi: 10.1016/j.nimb.2013.08.046.

2. L.J. Mao, J.C. Yang, D.Q. Gao, et al., Status of the HIAF Accelerator Facility in China[C]. RuPAC2021, Alushta, Russia. Doi:10.18429/JACoW-RuPAC2021-TUX01. R. Schmidt, R. Assmann, E. Carlier, et al., Protection of the CERN Large Hadron Collider[J]. New Journal of Physics 8, 2006(290): 31p. Doi:10.1088/1367-2630/8/11/290.

method for locking states and an algorithm for saving beam data. The method could realize the state locking of 25 monitored quantities and the saving of beam data up to 8.192ms. That also could meet the preservation of injector single pulse waveform data in the HIAF injection mode. The system was verified online in March 2024 through the state locking function, realizing real-time interlocking and equipment protection of beam position and beam intensity. The saving of interlock data was similarly tested in the laboratory, including sine wave and cumulative number. Due to the limitation of BRAM resources in hardware platform, this method could only store beam data for about 8ms. The next work is to develop the DDR-based data storage function,