Developing a new Beam Position Monitor Electronics For HIPA, the PSI High Intensity Proton Accelerator

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Abstract

The High Intensity Proton Accelerator (HIPA) at PSI presently has a radio frequency (RF) beam position monitor (BPM) system based on 20-year-old Xilinx Virtex-2 Pro Systems-on-Chip (SoC), using application-specific integrated circuits (ASICS) for direct digital downconverters. For the planned upgrade of the electronics as well as for new HIPA projects, we started the development of a new HIPA BPM electronics, using a generic electronics platform called "DBPM3" that is already being used for SwissFEL and SLS 2.0 electron BPM systems. In this contribution, first test results of a DBPM3-based HIPA BPM electronics prototype are presented, including a comparison with the present electronics.

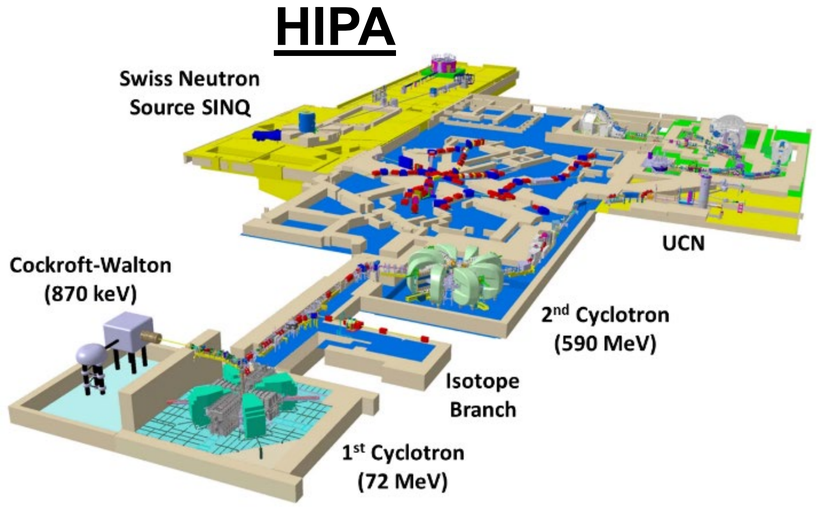
Machine Parameters

- Cockcroft-Walton Pre-accelerator: 870 keV CW
- 1st cyclotron: 72 MeV
- 2nd cyclotron: 590 MeV
- 2.4 mA max. beam current
- 1.4 MW max. CW beam power

BPM Pickups

- Two opposite coil with 1 winding as electrodes in beam pipe
- Horizontal and vertical coil pairs at different longit. positions
- Large beam pipe and geometry factors k = 37mm … 43 mm
- X = 37 mm * ($V_{right} – V_{left}$) / ($V_{right} + V_{left}$)
- Y = 37 mm * ($V_{top} – V_{bottom}$) / ($V_{top} + V_{bottom}$)

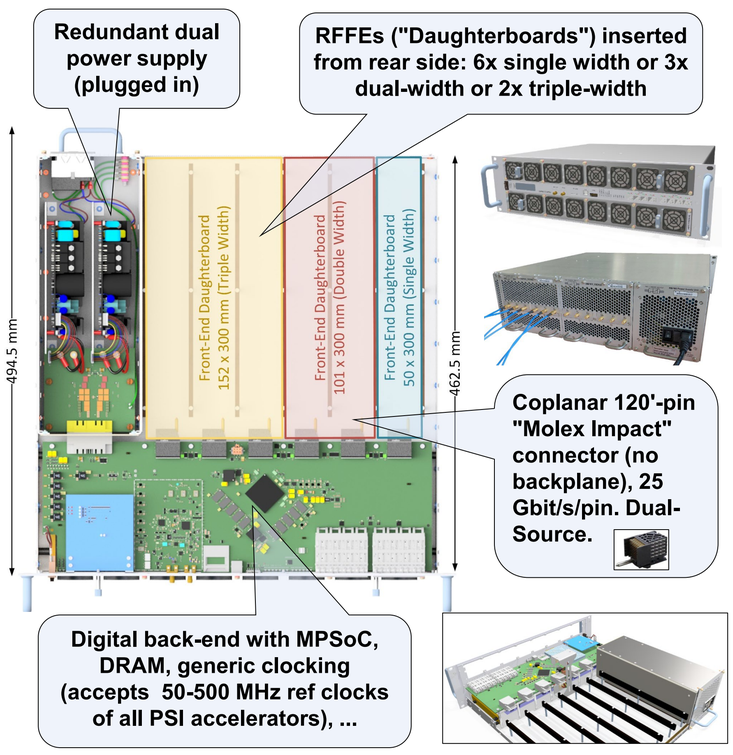
HIPA



BPM Specifications

Parameter	Specification
Beam Current Range	1-4000 µA
Pos. Noise < 5 Hz	< 0.1 mm (1-10 µA) < 0.03 mm (0.01-2 mA)
Pos. Noise < 20 kHz	< 0.2 mm (0.1-2 mA)
Pos. Dependence on Beam Current	< 0.5 mm (ramp from 5 µA to 2 mA)

DBPM3 Mechanical Concept

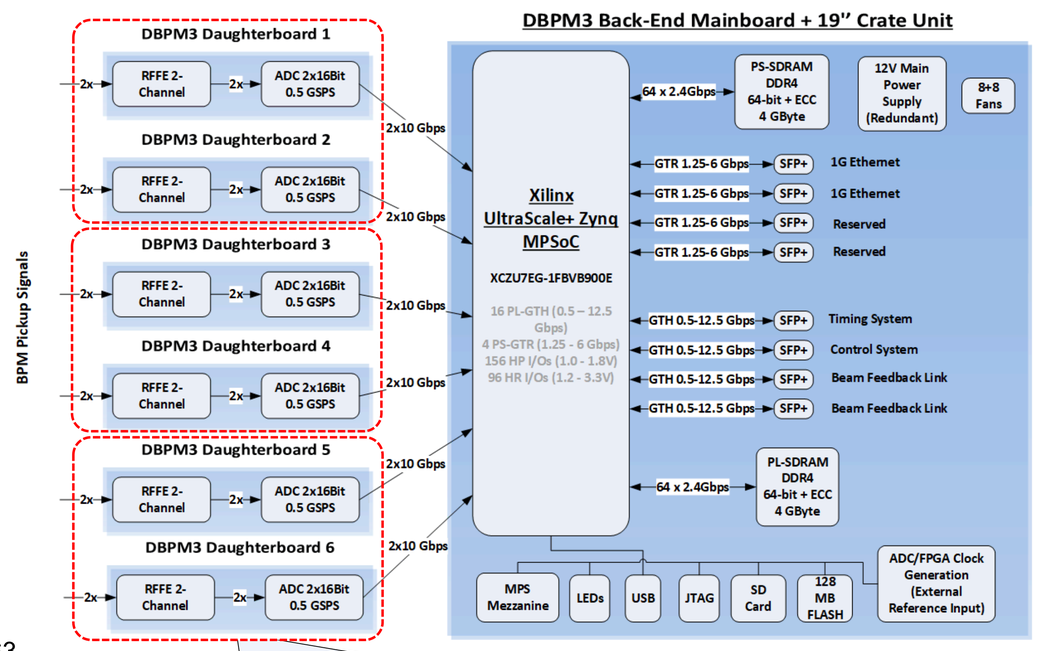


Digital Back-End with MultiProcessing System-on-Chip

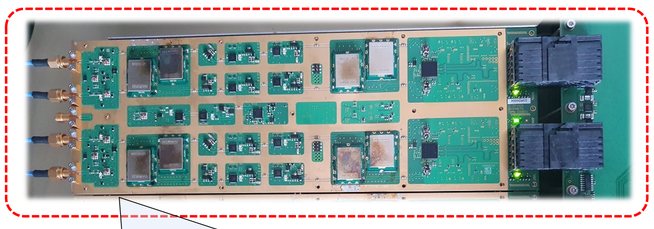
- Xilinx/AMD **Zynq UltraScale+** ("ZynqU+")
- 4-core 64-bit ARM CPU ("APU") running Linux/EPICS
- 2-core 32-bit ARM CPU ("RPU") running FreeRTOS (real-time DSP, ...)
- Two 72-bit DRAM banks (one for Linux, one for ADC real-time data stream)
- Already used for SwissFEL cavity BPMs and SLS 2.0 button BPMs

HIPA DBPM3 RF Front-End (RFFE) Electronics

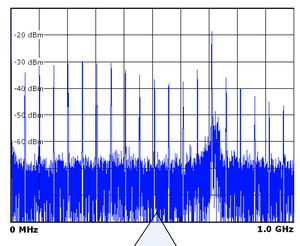
- 101.26 MHz beam signal (1st harmonic, beam bunched at 50.63 MHz)
- 63dB gain range
- RF front-end (RFFE) with integrated **ADC** (ADS54J69: **2-channel 16-bit 500 MSamples/s, JESD204B 10Gbps** serial interface)
- ADC now runs @ ~495 MS/s
- Digital DownConverter (DDC) implemented by PSI on Zynq UltraScale+, reprogramming of decimation rate and bandwidth during operation with GUI
- **3 simultaneous data streams (typ. 1 MSPS, 20 kSPS, 20 SPS)**



HIPA: Three RF Front-End daughterboards per DBPM3 unit, 4 channels each. JESD204B 16-bit 500Msps ADC (ADS54J69) integrated on RFFE.



HIPA RFFE prototype: PCB layout identical to new SLS electron button BPM electronics, but some different components soldered.

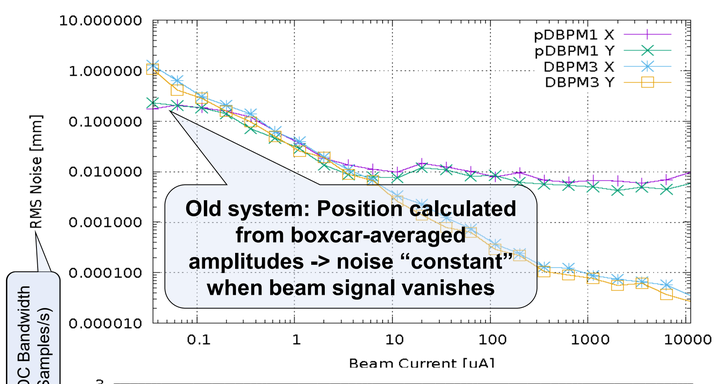


Beam signal spectrum: 50.63 MHz and harmonics

HIPA DBPM3 Performance

Comparison with present 20'-year old "pDBPM1" system:

- Lower noise at high beam current (better ADC, crossbar switch, more DDC bits)
- Similar noise at lower beam current (-> thermal noise limit, not much to improve)
- Better at very low current (DBPM3 ADC locked to accelerator RF: Boxcar averaging of old system replaced by narrowband DDC)

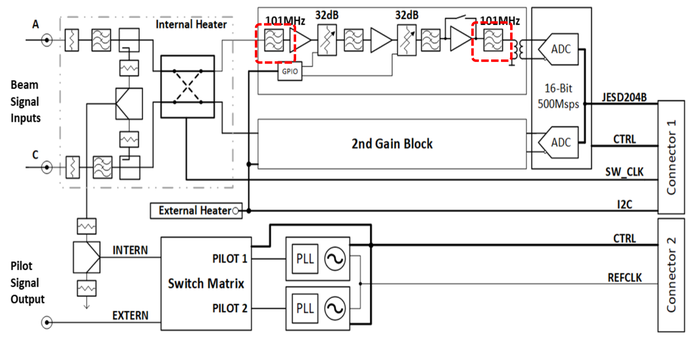


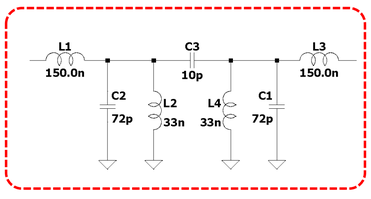
DDC Bandwidth	RMS Position Resolution
0.5 MHz (@1 MSPS)	<0.15 mm (0.1 mA) <0.03 mm (2 mA)
3 kHz (@20 kSPS)	<0.012 mm (0.1 mA) < 0.003 mm (2 mA)

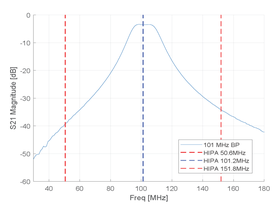
Measured DBPM3 broadband position noise

HIPA RFFE Schematics

- Re-used PCB from SLS 2.0 electron BPM RFFE, but adapted frequency-dependent parts
- Prototype: Self-made compact 101.26 MHz bandpass to fit PCB footprint of SLS 500 MHz bandpass
- Final version: New PCB layout, maybe slower/cheaper ADC, commercial bandpass with larger footprint







Motivation

- Age of present system (~20 years)
  - Using Xilinx Virtex-2 Pro: Obsolete design tools
  - Obsolete hardware parts
  - Limited number of spares
- Need for additional BPMs
  - "IMPACT" project: Extension of HIPA facility for production of isotopes & high-intensity muon beam
- Present RF-front end (radiation-hard) in accelerator bunker (only ADC/back-end outside)
  - RFFEs activated, want to avoid dose rates for personnel during maintenance
  - New DBPM3 electronics will be completely outside bunker, needs new RF cables

Summary & Outlook

- The present DBPM3 prototype hardware performance already meets HIPA requirements
- Next steps:
  - RFFE PCB redesign to fit COTS bandpass & optimize costs (ADC could be slower/cheaper, …)
  - DBPM3 for smaller number of new BPMs (2027: First beam for new IMPACT project)
  - Replace all electronics & RF cables (2028+)