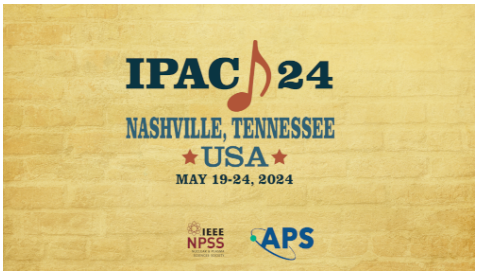

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EPICS communication structure based on a SoC FPGA board

Thursday, 23 May 2024 16:00 (2 hours)

In the radio frequency system of a synchrotron accelerator, precise modulation of signals in the radio frequency cavity is crucial for achieving a stable acceleration electric field. The National Synchrotron Radiation Research Center's (NSRRC) Taiwan Photon Source (TPS) underwent a significant upgrade in 2019, transitioning from analog to digital control for the low-level radio frequency system. This upgrade enhances noise resistance and enables more precise control. Within the NSRRC's digital low-level radio frequency control system, a Field-Programmable Gate Array (FPGA) serves as the core, interfacing with a Raspberry Pi through GPIO to connect to the Experimental Physics and Industrial Control System (EPICS). This article outlines the implementation of a SoC FPGA, constructing a Linux OS within the Hardware Process Structure (HPS), and establishing direct communication with EPICS.

Footnotes

Funding Agency

Paper preparation format

Region represented

Asia

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