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FPGA design of FRIB chopper monitor system

Thursday, 23 May 2024 16:00 (2 hours)

In FRIB we use chopper in the low energy beam line for beam power controls. As appropriate functioning of chopper is critical for both beam operation and machine protection, an FPGA-based chopper monitoring system was developed to monitor its operation for fixed duty cycle operation and has been in use to support operation. The chopper monitor shuts off beam promptly at detection of a deviation of duty cycle outside tolerance. For future higher beam power operation, automatic beam power ramp modes will be required where beam duty factor is dynamically ramped up following a predetermined sequence. Recently FPGA prototype is developed to enhance the chopper monitor to accommodate one of such dynamic modes, cold start beam mode. It is a design challenge to integrate all the beam modes in one FPGA while synchronizing with external timing system pulse generator and recording the process data and failure information. Detailed FPGA design for this enhancement of chopper monitor will be discussed in this paper, followed by the test result of integrated system of chopper monitor, global timing system pulse generator, high voltage switch of chopper control and EPICS control software.

Footnotes

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