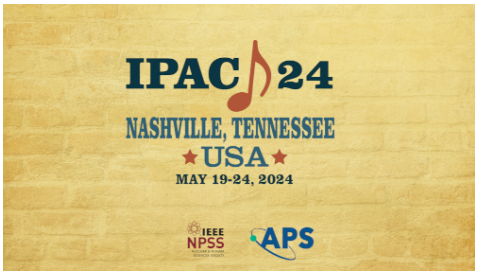

Contribution ID: **1038** Contribution code: **WEPG08** Type: **Poster Presentation**

NSLS-II bunch-by-bunch BPM development and beam operation

Wednesday, 22 May 2024 16:00 (2 hours)

The Radio Frequency System-on-Chip (RFSoC) FPGA-based high-performance bunch-by-bunch beam position monitor (BxB BPM) was developed and commissioned at NSLS-II. The new BxB BPM features a 14-bit 5 Gsps ADC, directly sampling 2 ns four-button signals, and digital signal processing with a synchronized 500 MHz RF reference clock. The BxB BPM provides 32 K points of ADC raw data, 5 K turns for up to 1320 bunch amplitude and position data, 2.6 million turn-by-turn (TxT) data points, 10 K turns of circular buffer, and 10 Hz streaming data. The potential applications include, but are not limited to measuring injection transient, efficiency, ion instability detection, and single/multi-bunch motion analysis. A ˜15 µm single-bunch resolution was confirmed with the beam test. This paper will present the beam test results, hardware FPGA firmware architecture, and control system interface for operation.

Footnotes

Funding Agency

U.S. Department of Energy (DOE) Office of Science under Contract No. DE-SC0012704.

Paper preparation format

Word

Region represented

North America

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Session Classification: Wednesday Poster Session

Track Classification: MC6: Beam Instrumentation, Controls, Feedback, and Operational Aspects: MC6.T03 Beam Diagnostics and Instrumentation