

Contribution ID: 1922 Contribution code: MOCN2 Type: Contributed Oral Presentation

Direct RF sampling based LLRF control system for C band linear accelerator

Monday, 20 May 2024 15:20 (20 minutes)

Low Level RF (LLRF) control systems of linear accelerators (LINACs) are typically implemented with heterodyne based architectures, which have complex analog RF mixers for up and down conversion. The Gen 3 RF System-on-Chip (RFSoC) device from AMD Xilinx integrates data converters with maximum RF frequency of 6 GHz. That enables direct RF sampling of C band LLRF signal typically operated at 5.712 GHz without RF mixers, which can significantly simplify the system architecture. The data converters sample RF signals in higher order Nyquist zones and then up or down converted digitally by the integrated data path. The closed-loop feedback control firmware implemented in FPGA integrated in RFSoC can process the baseband signal from the ADC data path and calculate the updated phase and amplitude to be up-mixed by the DAC data path. We have developed an LLRF control RFSoC platform, which targets Cool Copper Collider (C3) and other C or S band LINAC research and development projects. In this paper, the architecture of the platform and the test results for some of the key performance parameters, such as phase and amplitude stability with our custom solid-state amplifier, will be described.

Footnotes

Funding Agency

Paper preparation format

LaTeX

Region represented

North America

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Session Classification: MOCN: Beam Instrumentation, Controls, Feedback and Operational Aspects (Contributed)

Track Classification: MC6: Beam Instrumentation, Controls, Feedback, and Operational Aspects: MC6.T27 Low Level RF