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Development of a new digital LLRF system for high energy photon source

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A new digital low-level RF (LLRF) system has been developed for the High Energy Photon Source (HEPS), a 6 GeV diffraction-limited synchrotron light source under construction in Beijing. The system is composed of a digital signal processing board (DSP), two ADC/DAC daughter boards and a RF front-end board. The FPGA of the DSP board has been changed from the original ALTERA Stratix III to Xilinx zynq-7000 which comes with a versatile Processing System (PS) integrated with a highly flexible and high-performance Programmable Logic (PL) section, all on a single System on Chip (SoC). The control algorithms were implemented in PL section while the EPICS-IOC was running on the embedded Xilinx Linux within the PS. The LLRF system has been tested with a 166.6 MHz mockup cavity in the lab and the RF field inside the cavity can be controlled within +/-0.02% in amplitude error and +/-0.02 degree in phase error (peak to peak). The requirements of HEPS were therefore fulfilled. The hardware design, control algorithms and the test results of the new LLRF system are described in this paper.

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