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Tuner loop based on FPGA for Petra cavity at TPS booster ring

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The low level RF system of TPS booster ring was replaced by the DLLRF in 2018. After that, the phase drift compensation loop for energy saving operation and the tuner loop were also implemented into the DLLRF system sequentially. We used altera-DE3 to build the core of DLLRF and to handle the high speed ADC/DAC procedure for RF signal sampling. As facing to the tuner control requirement, we choose an another low cost board, altera-DE0-Nano, to develop the tuner loop for 5-Cells-Petra-Cavity. It has an eight channels 12-bits-ADC, ADC128S022, to detect two tuners' positions and two transmit powers for power balance function. The phase information of forward power and cavity gap voltage will get from altera-DE3 to tell the tuner loop in altera-DE0-Nano that the cavity is resonance or not. The tuner loop controls the cavity to work not only at resonance frequency but also with balance electric field distribution. In this study, the architecture of the tuner loop is presented including locking resonance frequency and field balance functions. The performance of field balance function is observed by the archive data of two tuners' positions and two transmit powers.

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Footnotes

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Yes

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