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Digital LLRF feedbacks development, implementation and test at KEK LUCX facility

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High Demand for stability, accuracy, reproducibility and monitoring capability were placed on accelerators LLRF systems, because of fundamental and applied experimental requirements. Meanwhile, availability of FPGA boards became better during last two decades. Nowadays, it is possible to implement FPGA based LLRF feedback using boards with S-band (or L-band) ADC&DAC (direct sampling technique) or boards with low-bandwidth ADC&DAC up to 60MHz (down-conversion technique).

If FPGA board with S-band or L-band ADC&DAC is not available, there are two options to implement feedback into the LLRF system. Both of them operate in down-conversion mode.

The first option employs external I/Q demodulator, I/Q signals digitization, phase and amplitude calculation, buffering into DDR memory, PI feedback, I/Q modulation and RF signal regeneration. This approach does not require an expensive, highly stable slave oscillator or slave signal generator to down-convert picked-up signals from RF cavity. However, the external I/Q demodulator has to be properly examined to define the phase and amplitude detection resolution.

The second option is almost the same, but I/Q demodulator is implemented into the FPGA logic. Picked RF signal frequency has to be down-converted with slave oscillator or slave signal generator.

Both approaches were implemented and tested at KEK LUCX facility. This report presents feedbacks' performance results. Also, technical details are discussed.

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Footnotes

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Yes

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