An Ultra-Low Latency ATCA-based Data Acquisition Platform for Real-time Beam Current Monitoring and Fast Protection at CSNS-II

Peng Zhu

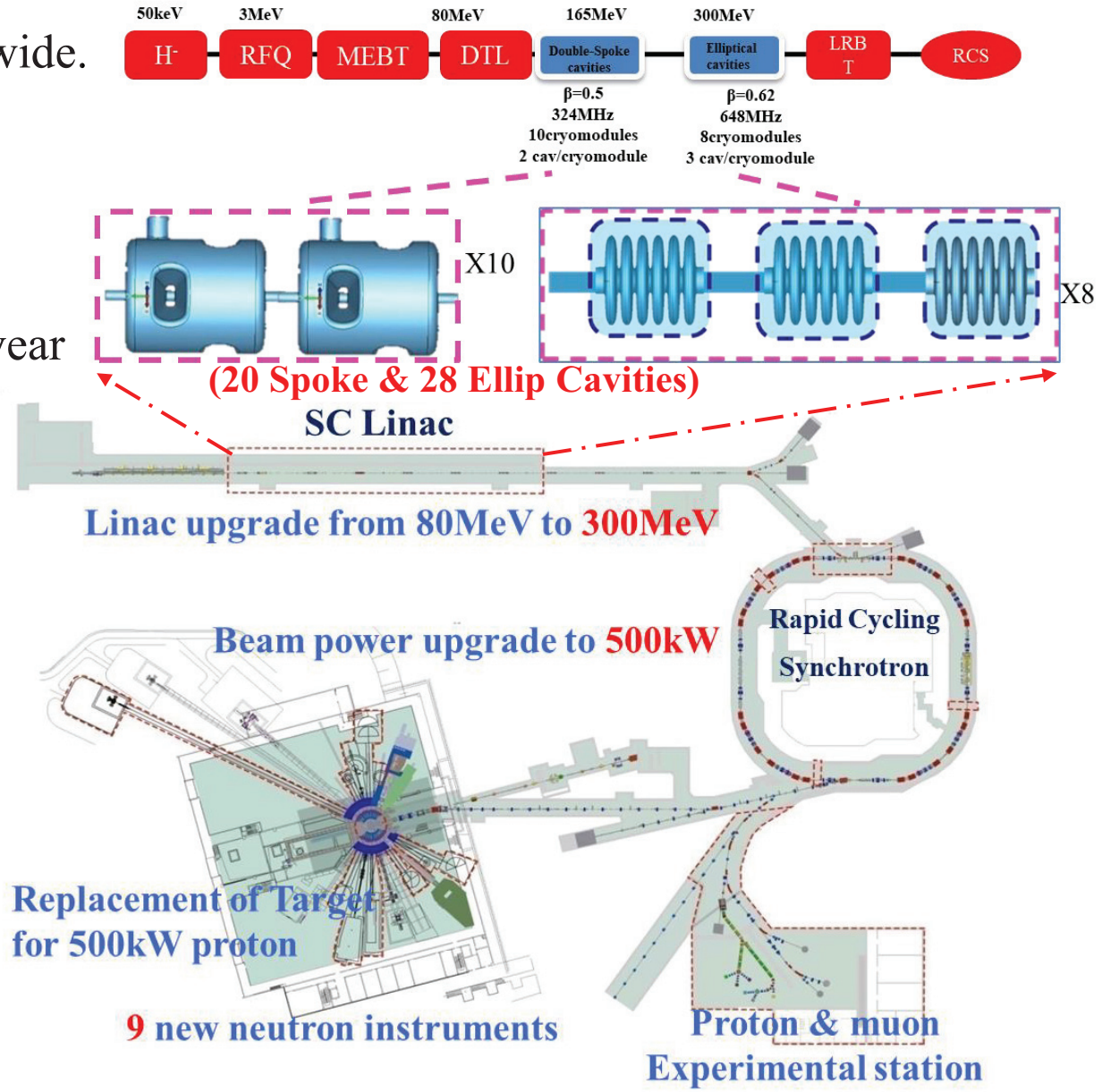
The 15th International Beam Instrumentation Conference (IBIC), Canada

Outline

- Background & Requirements
- Design and Implementation of ATCA-Based Hardware
- Experimental Validation of the DBCM Prototype
- Future Work
- Summary

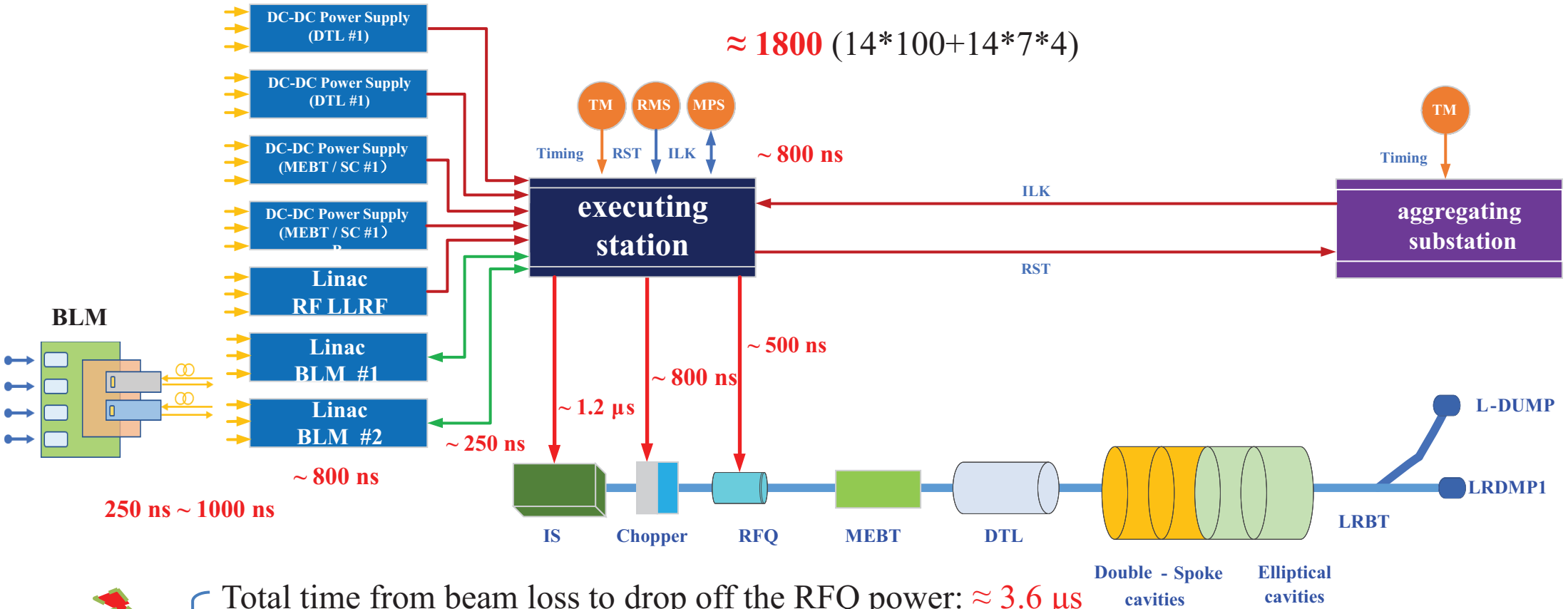
Overview of the Linac

- The fourth pulsed spallation neutron source worldwide.
- National acceptance on August 23, 2018.
- Operating efficiently and stably for seven years.
- Upgrade approved in 2024, with an estimated six-year construction period.
  - ➢ Phase I: 80 MeV, running now.
  - ➢ Phase II: 300 MeV, preparation.



Requirements & Architecture for Fast Protection System

- **The FPS for Linac** (Distributed System, A key component of the accelerator)
  - Each substation independently connects to 100 interlocking signals.
  - Each Rocket IO channel processes 16 signals, and the maximum number of signals that the master station can handle：

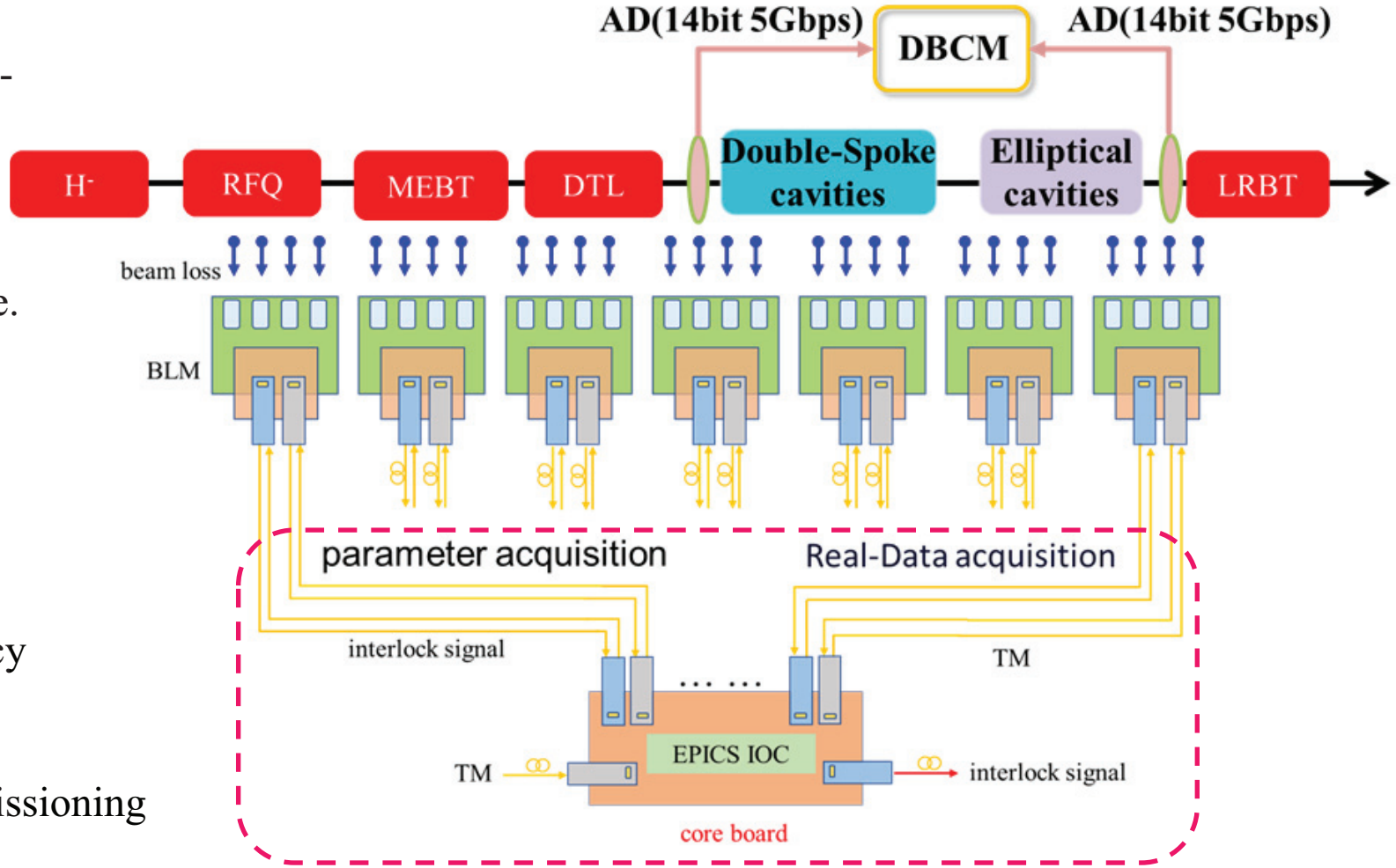


Total time from beam loss to drop off the RFQ power: ≈ 3.6 µs
Total time from beam loss to shutdown timing of the chopper: ≈ 4 µs
Total time from beam loss to shutdown timing of the ion source extraction power supply: ≈ 4.5 µs

Function for ATCA-based Data Acquisition Platform

- **Integrate FPS & TM:** Provide real-time beam data with high-precision timestamps for beam commissioning and machine studies.

  - ✓ Synchronously acquire bunch-by-bunch beam data.
  - ✓ Perform real-time analysis and decision-making to minimize machine protection response time.
  - ✓ Utilize Edge AI to determine the optimal timing for beam stop.



- **Challenges**

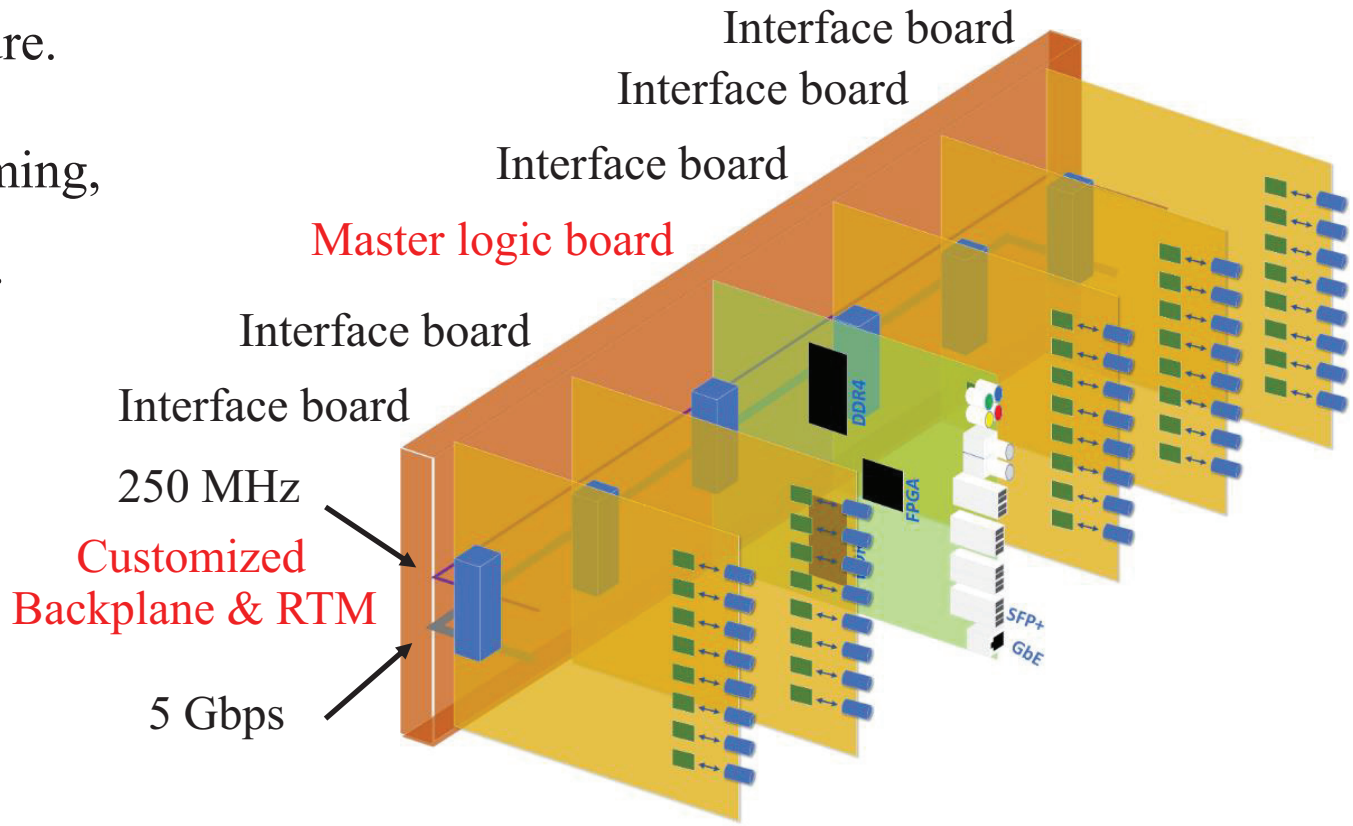
  - ➢ Ultra-high reliability and accuracy
  - ➢ High-precision timestamps
  - ➢ Signal integrity and beam commissioning

Hardware for ATCA-based Data Acquisition Platform

- **Motivation:** (1) VME --> xTCA.
  (2) demo FPGA --> RAM + Linux + EPICS (Embedded IOC).
  (3) distributed data --> Associated data with high-precision timestamps (EVR).
- **Approach: ATCA + FPGA + Rocket I/O**

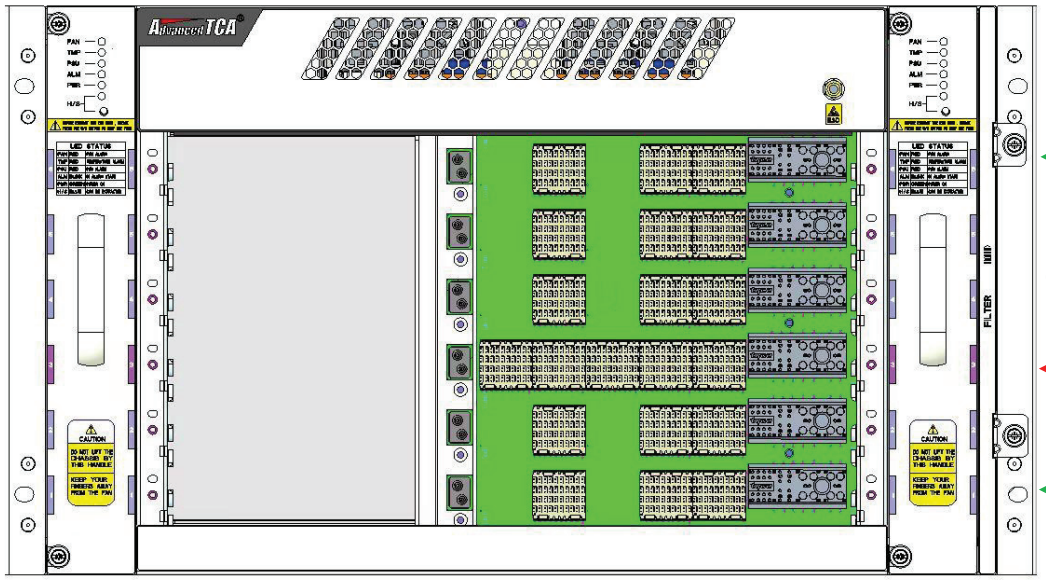
✓ Based on the ATCA mechanical architecture.

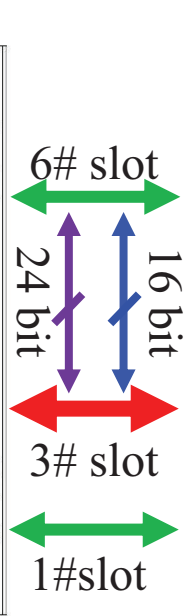
✓ Integrating functions of fast protection, timing, beam loss configuration, and data readout.

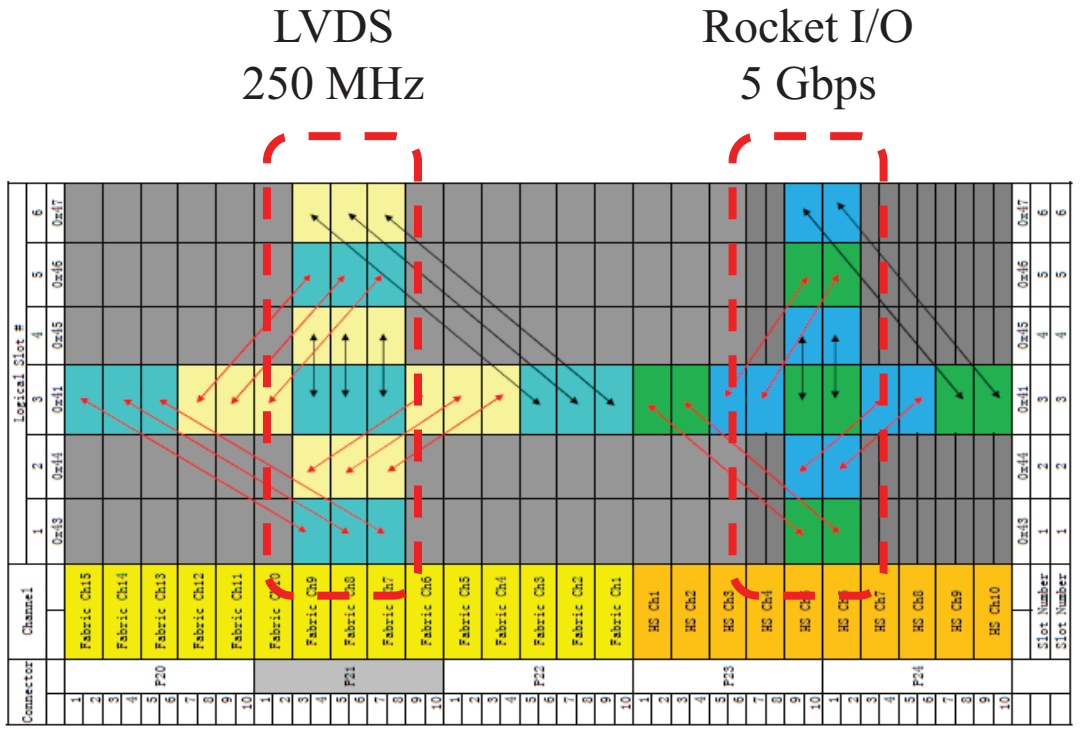


Hardware for ATCA-based Data Acquisition Platform

■ Self-developed backplane with signal interfacing







- ✓ **Master**: slot #3, while slave: slots #1, #2, #4, #5, and #6.
- ✓ **Master slot** handles logical processing, parameter configuration, status readback, and on-board IOC.
- ✓ **Slave slots** handle external signal input and internal signal output.
- ✓ Master slot is directly connected to each slave slot via 32 pairs of high-speed differential signals through pin-to-pin routing on the backplane.

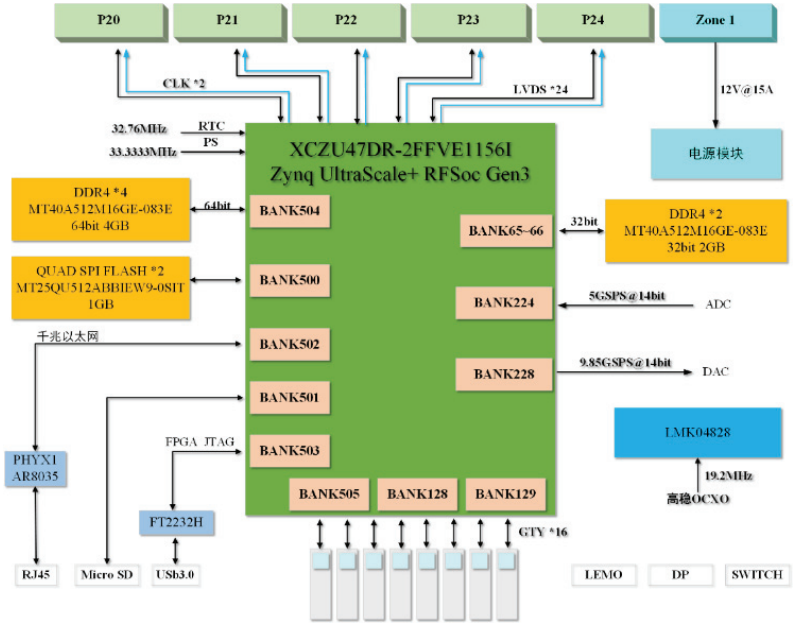
Hardware for ATCA-based Data Acquisition Platform

- **System Components: Master logic board, Self-developed backplane, and Interface boards**

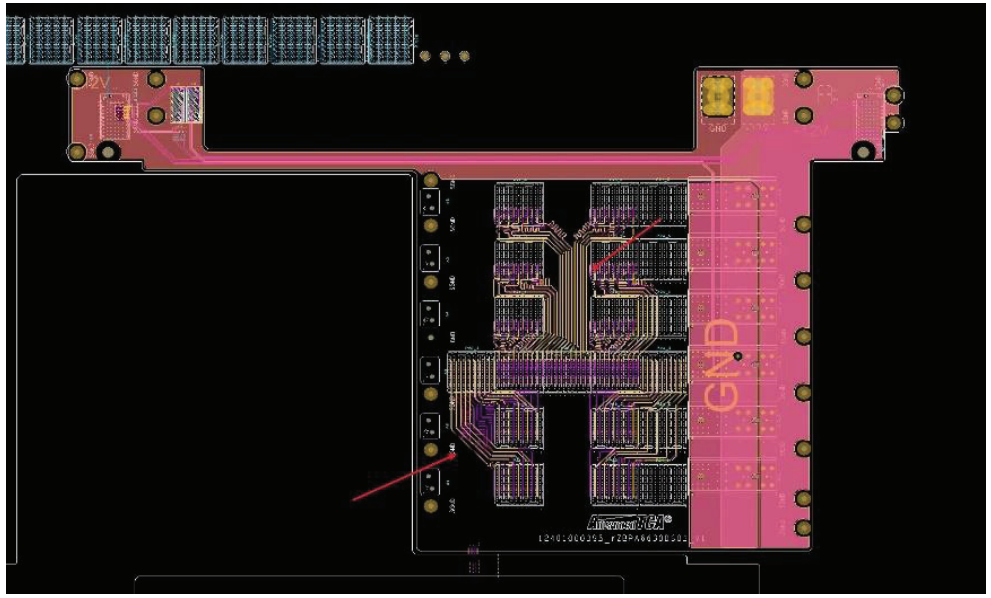
- **Master logic board:** Acquisition & Signal processing & Interlock logic
  - ✓ RF SoC: real-time ADC acquisition and beam signal processing.
  - ✓ KU060: interlock logic and beam abort via point-to-point links to interface boards.

32-bit LVDS parallel bus
RF SoC interface with KU060

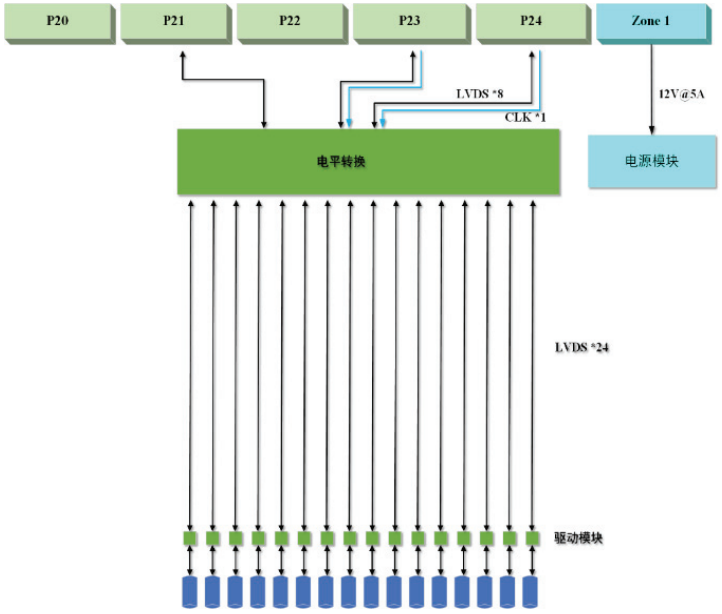
- **Interface boards:** Signal I/O with external subsystems



RF SoC (Master logic board)



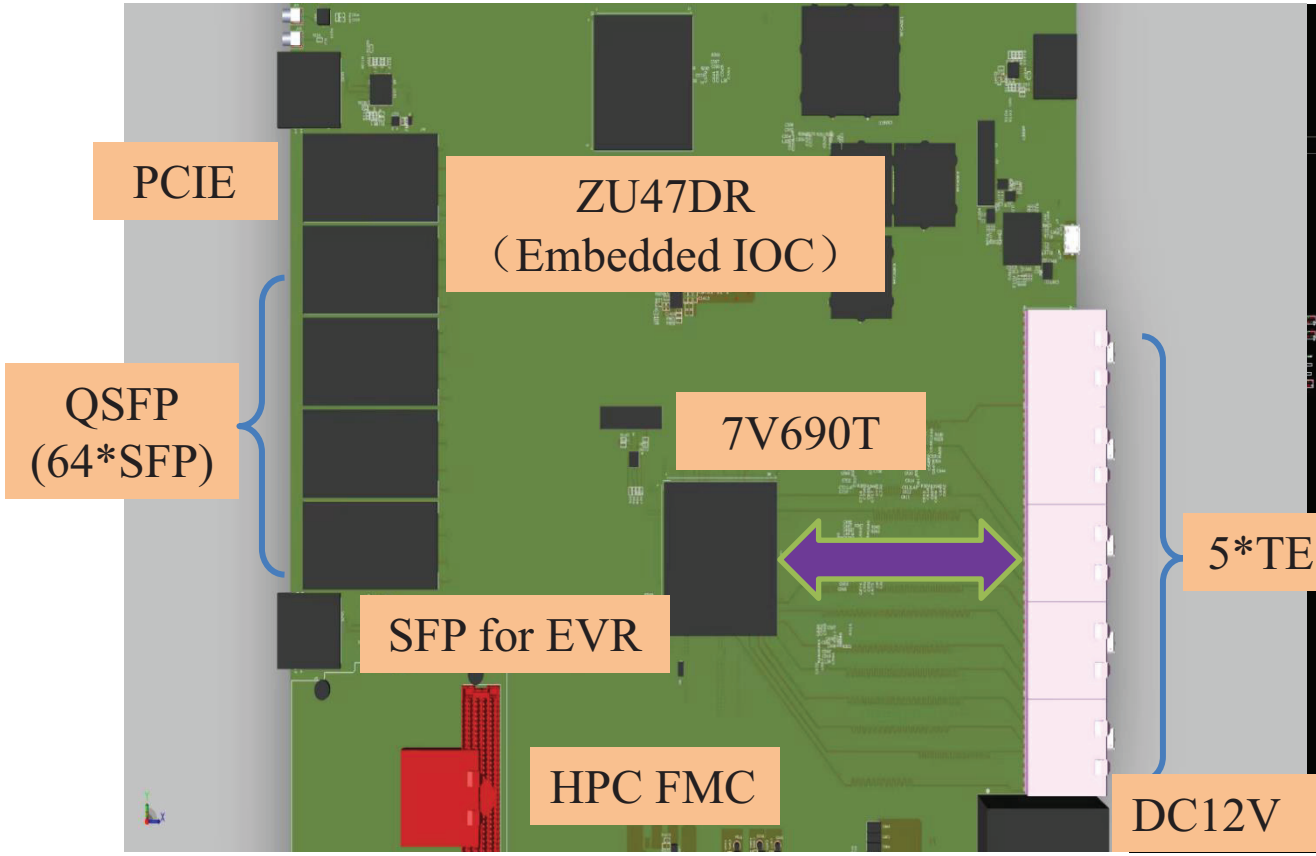
Self-developed backplane
(no logic chip, just point-to-point links)



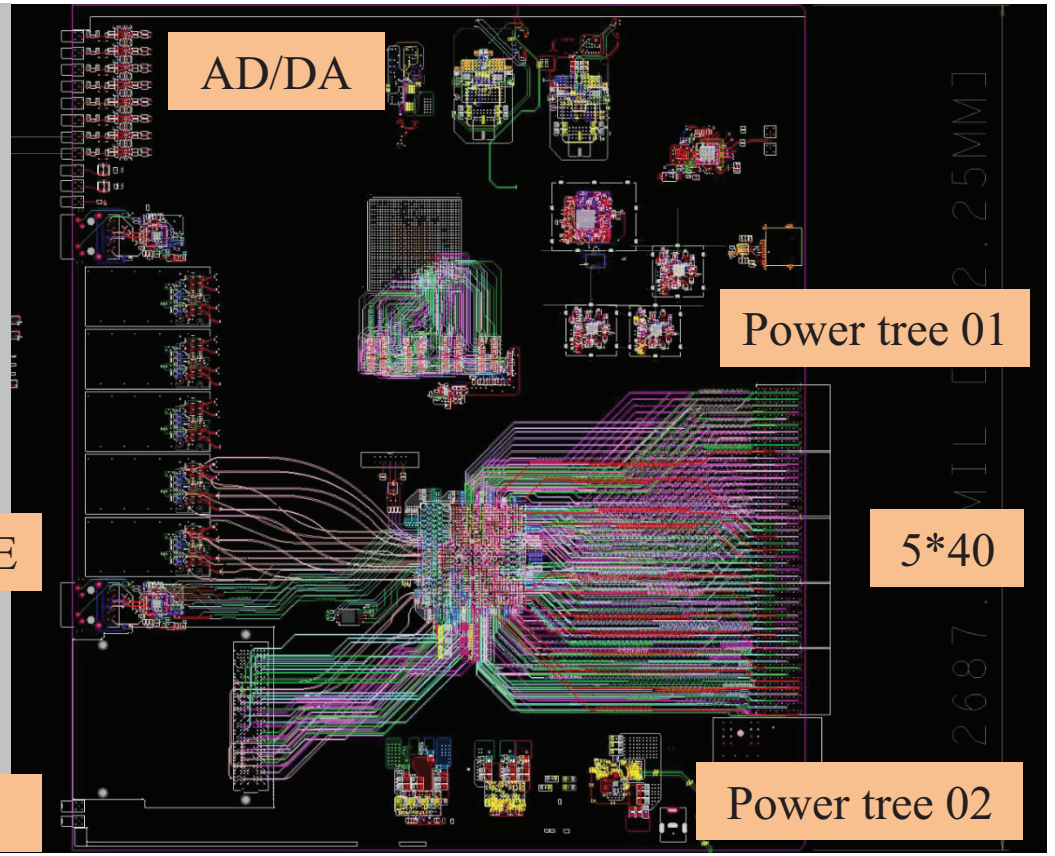
Interface board
(no logic chip, just basic Functions)

Hardware for ATCA-based Data Acquisition Platform

- **Master logic board:** Completed schematic and PCB design, plus functional debugging of the 6U ATCA core master logic board.
  - 4 QSFP + 1 PCIE
  - Event timing support
  - HPC FMC
  - 8 x 14 bits **ADC, 5 GSPS, 6GHz** analog BW
  - 8 x 14 bits **DAC, 10 GSPS, 4GHz** analog BW
  - Megtron-6, 24 Layer



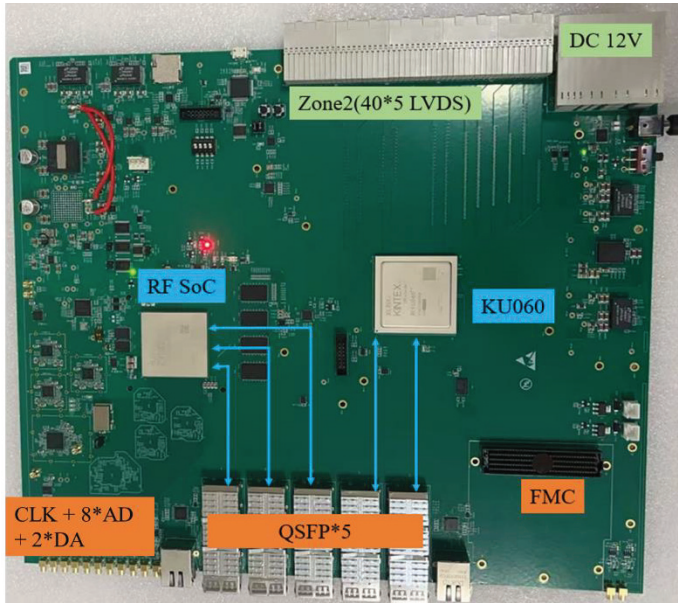
3D view

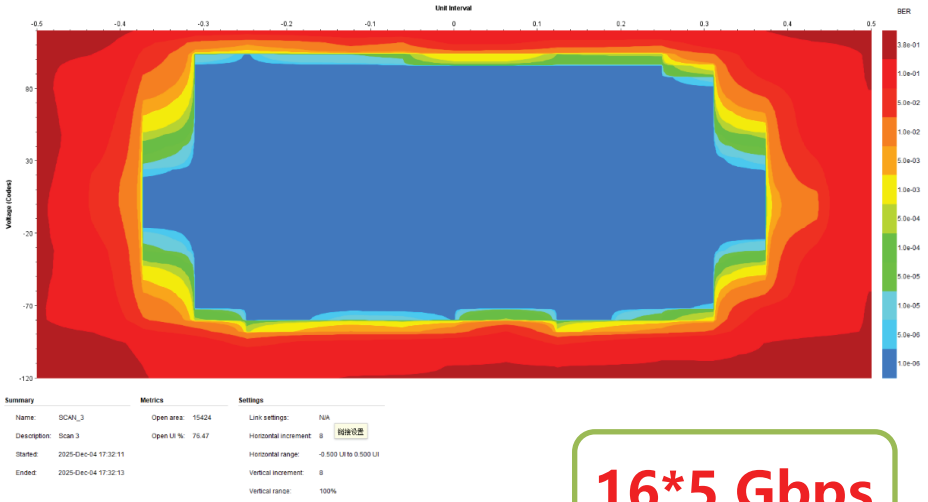


Layout

Hardware for ATCA-based Data Acquisition Platform

- **Master logic board:** Achieved error-free 5 Gbps high-speed transmission across 16 channels.





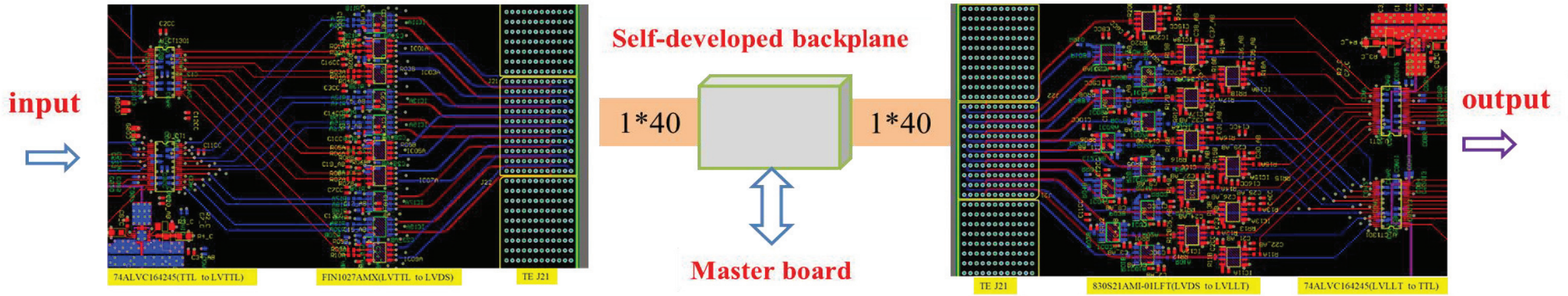
16*5 Gbps

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

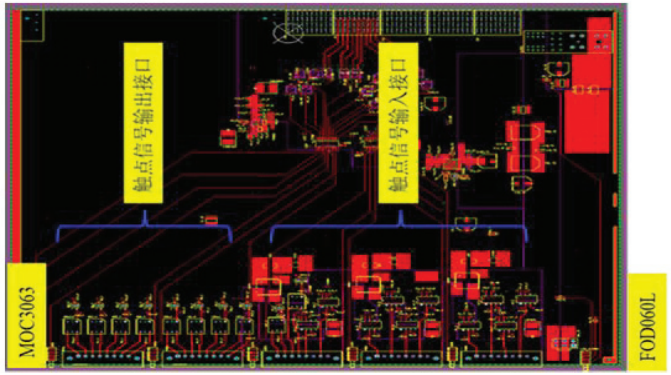
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mo
Ungrouped Links (0)																			
Found Links (8)							Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset			None
Auto detected link 0	Quad_228/MGT_X1Y16/TX (xcku060_0)	Quad_227/MGT_X1Y12/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 1	Quad_228/MGT_X1Y17/TX (xcku060_0)	Quad_227/MGT_X1Y13/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 2	Quad_228/MGT_X1Y18/TX (xcku060_0)	Quad_227/MGT_X1Y14/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 3	Quad_228/MGT_X1Y19/TX (xcku060_0)	Quad_227/MGT_X1Y15/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 4	Quad_227/MGT_X1Y12/TX (xcku060_0)	Quad_228/MGT_X1Y16/RX (xcku060_0)	5.014 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 5	Quad_227/MGT_X1Y13/TX (xcku060_0)	Quad_228/MGT_X1Y17/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 6	Quad_227/MGT_X1Y14/TX (xcku060_0)	Quad_228/MGT_X1Y18/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None
Auto detected link 7	Quad_227/MGT_X1Y15/TX (xcku060_0)	Quad_228/MGT_X1Y19/RX (xcku060_0)	5.000 Gbps	2.348E12	0E0	4.259E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (1100)	☑	Inject	Reset	Reset	Locked	Locked	None

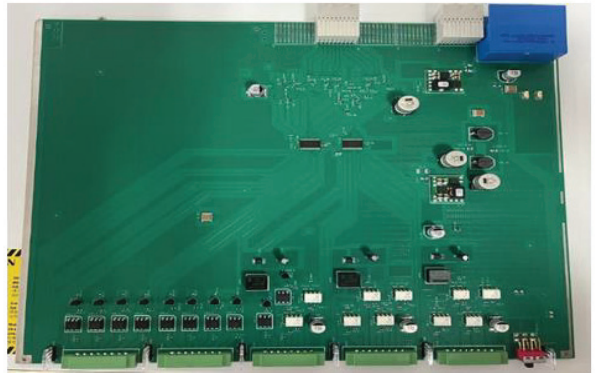
Hardware for ATCA-based Data Acquisition Platform

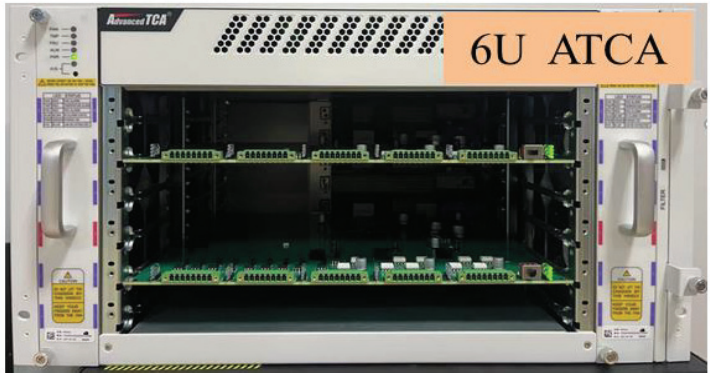
- **Interface board:** **Optical-type & PLC-type to cover different application.**
  - **Opt-type input :** HFBR2412T => 74ALVC164245 =>FIN1027AMX(LVTTL to LVDS) => TE
  - **Opt-type output :** TE => 830S21AMI-01LFT(LVDS to LVLLT)=> 74ALVC164245=> HFBR1414T



- **PLC-type input :** phoenix => FOD060L => 74ALVC164245=>FIN1027AMX(LVTTL to LVDS) => TE
- **PLC-type output :** TE => 830S21AMI-01LFT74ALVC164245(LVLLT to TTL) => MOC3063 => phoenix

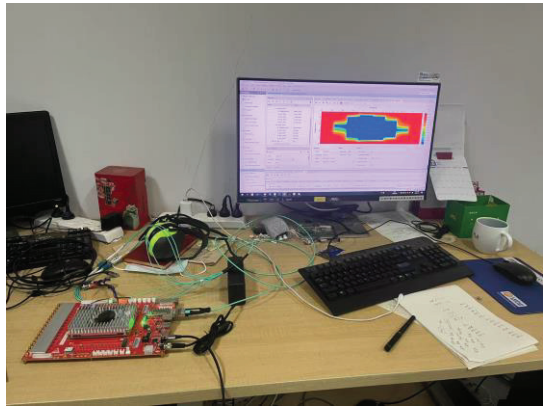






Hardware for ATCA-based Data Acquisition Platform

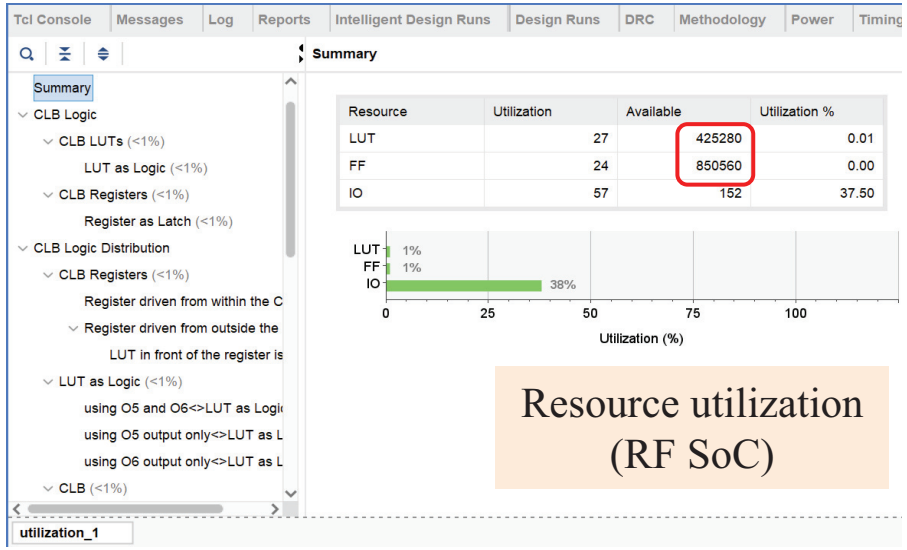
- **Current Status:** Porting of Fast Protection Firmware for online operation.



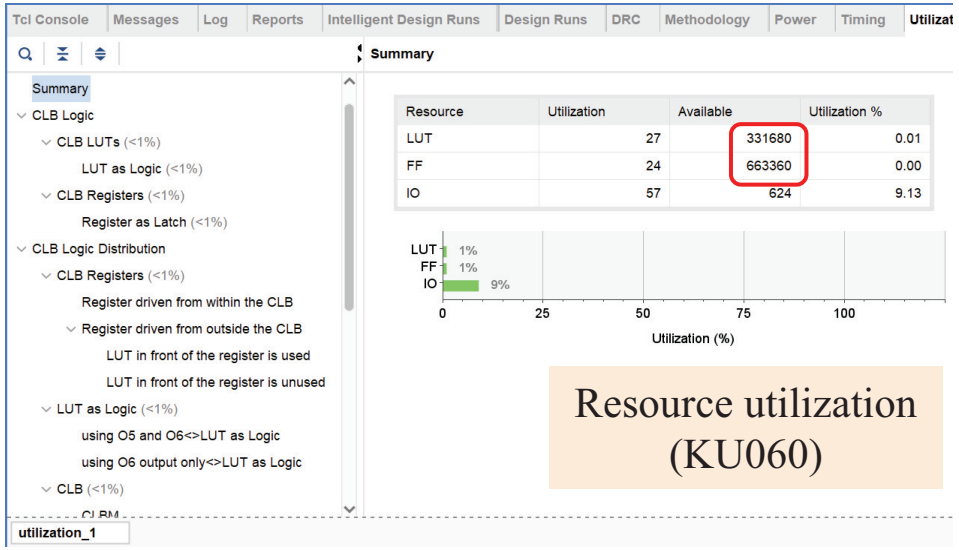
Implementation	Summary
Status:	✓ Complete
Messages:	! 3 warnings
Active run:	impl_1
Part:	xcku060-ffva1517-2-i
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

Implementation	Summary
Status:	✓ Complete
Messages:	! 3 warnings
Active run:	impl_1
Part:	xczu47dr-ffve1156-2-i
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

Both chips are fully integrated, with online beam commissioning targeted for early 2027.



Resource utilization (RF SoC)



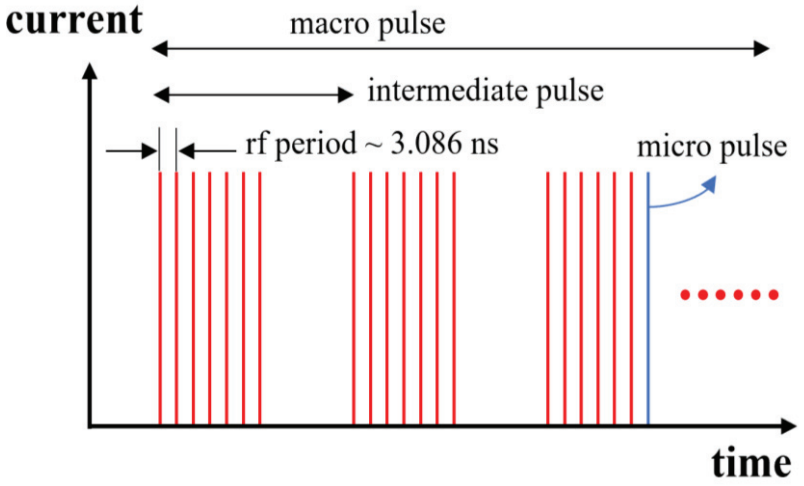
Resource utilization (KU060)

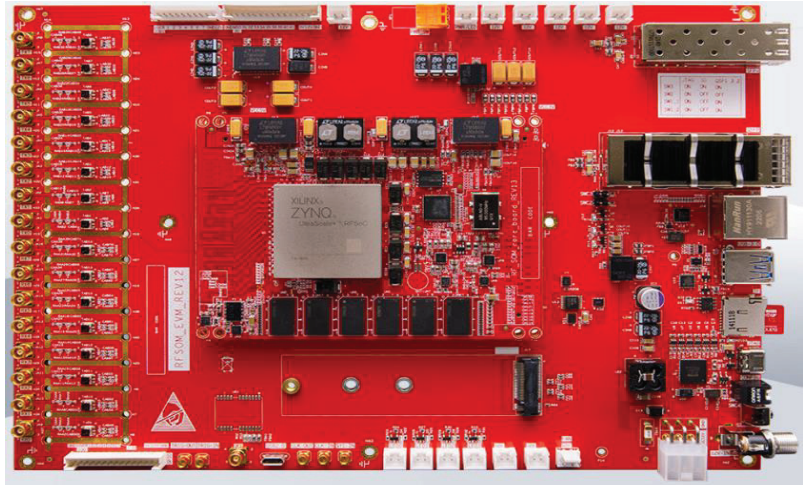
Outline

- Background & Requirements
- Design and Implementation of ATCA-Based Hardware
- **Experimental Validation of the DBCM Prototype**
- Future Work
- Summary

Experimental Validation of the DBCM Prototype

- **A prototype was developed to validate the RF SoC-based DBCM solution for real-time beam monitoring**





RF SoC Development Board Physical Diagram

- The minimum micro-bunch repetition rate is 324 MHz. An ADC with a sampling rate of at least 648 MSPS is required.
- The horizontal timing jitter of micro-bunches exceeds twice the RF period, making it highly susceptible to sampling inaccuracies.

- ✓ Seamless integration of ADC and ARM processors into a single chip.
- ✓ Supports high-speed signal acquisition up to 5 GHz, with highly efficient I/Q signal generation required for demodulation.
- ✓ Supports embedded Linux and upper-layer application development.

Experimental Validation of the DBCM Prototype

■ Signal Processing Architecture (No multi-device cascading & Low latency)

FCT → RF-ADC → Demodulation → Differential Calculation → Decision-making → Protection Output

➢ Signal Acquisition and Processing (PL)

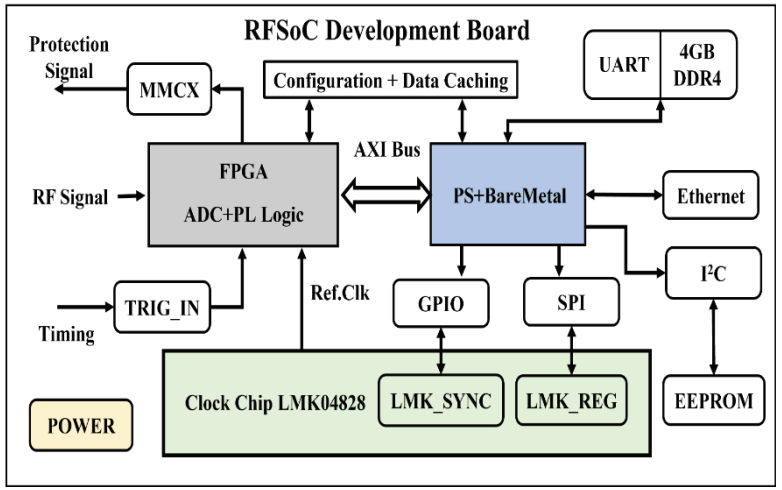
- ✓ Digitize incoming ADC signals.

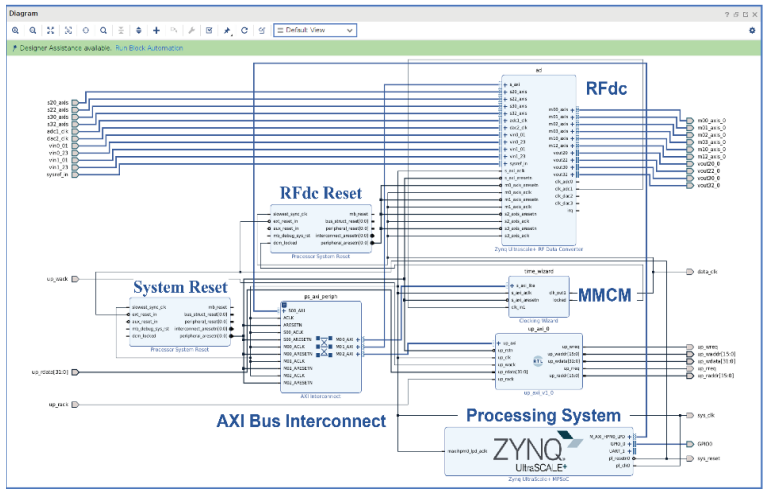
➢ Real-time Processing (PL)

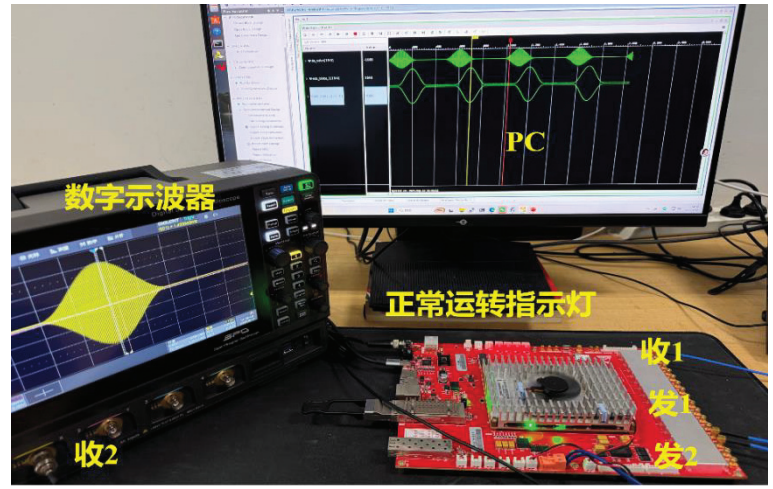
- ✓ Process the sampled data in real time to generate protection signals. Meanwhile, the data or status information is transmitted to the PS side via the AXI bus.

➢ Control and Communication (PS)

- ✓ A Linux application to handle system configuration and data buffering.
- ✓ Communicates with the host computer via Ethernet and storage devices via GPIO.

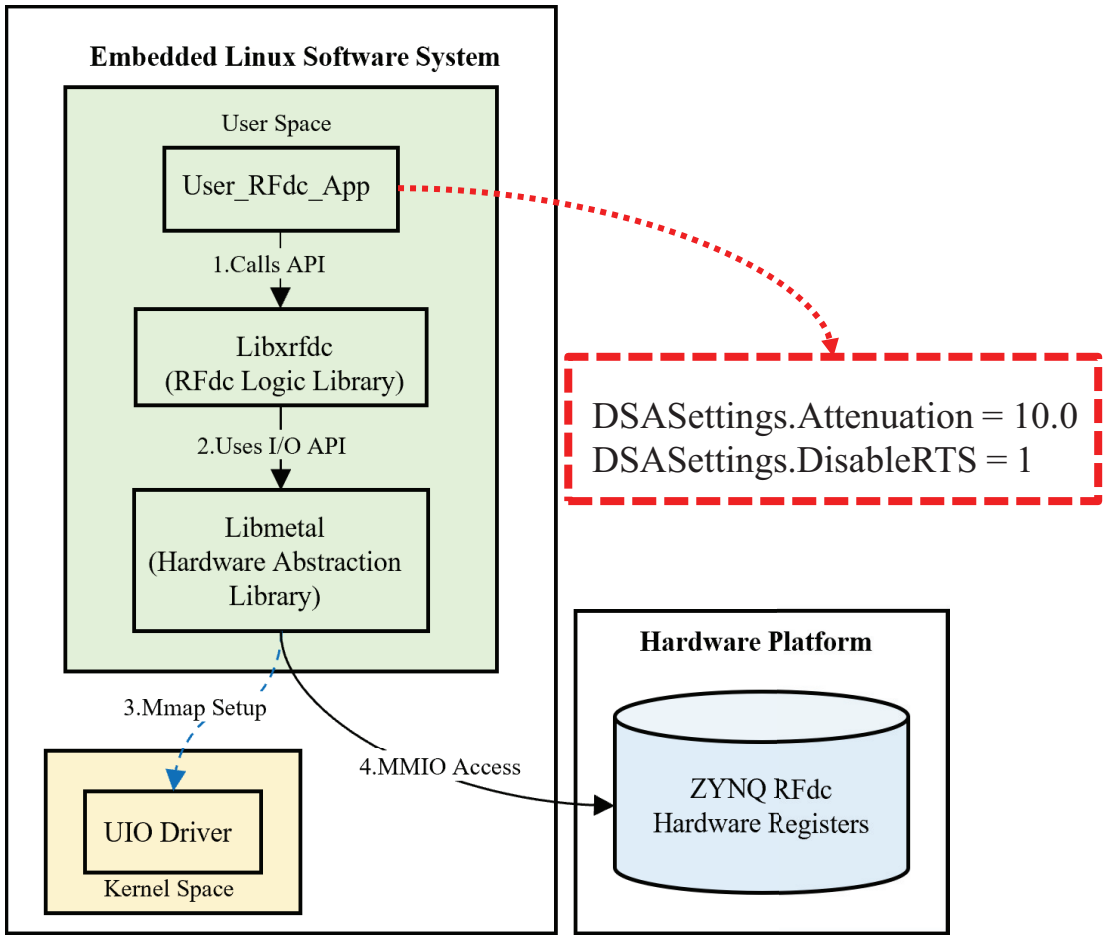






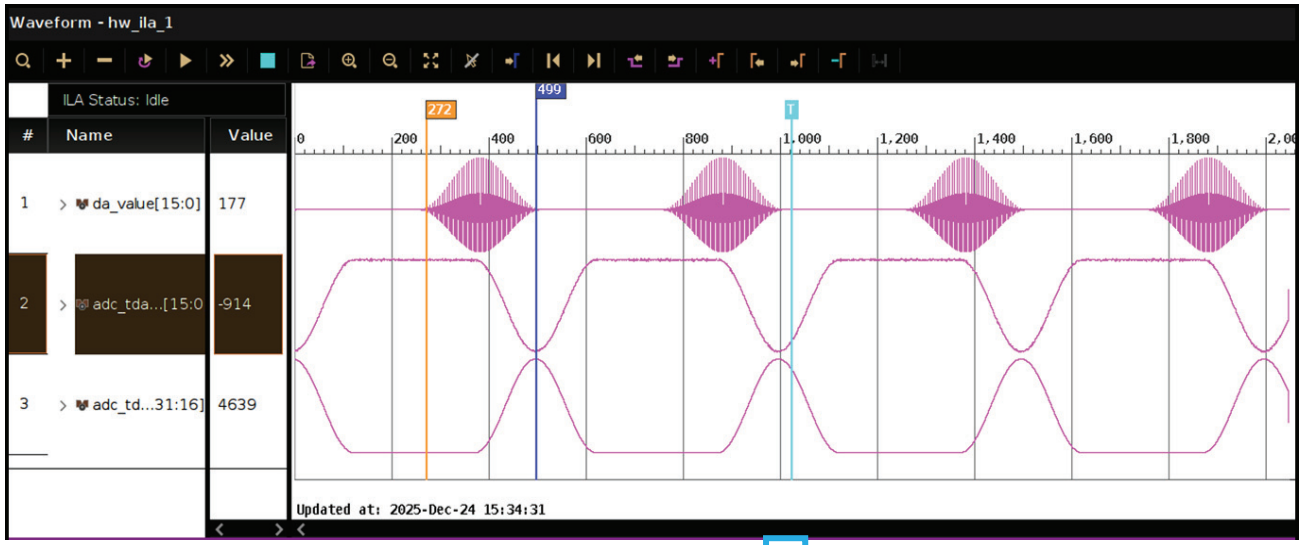
Experimental Validation of the DBCM Prototype

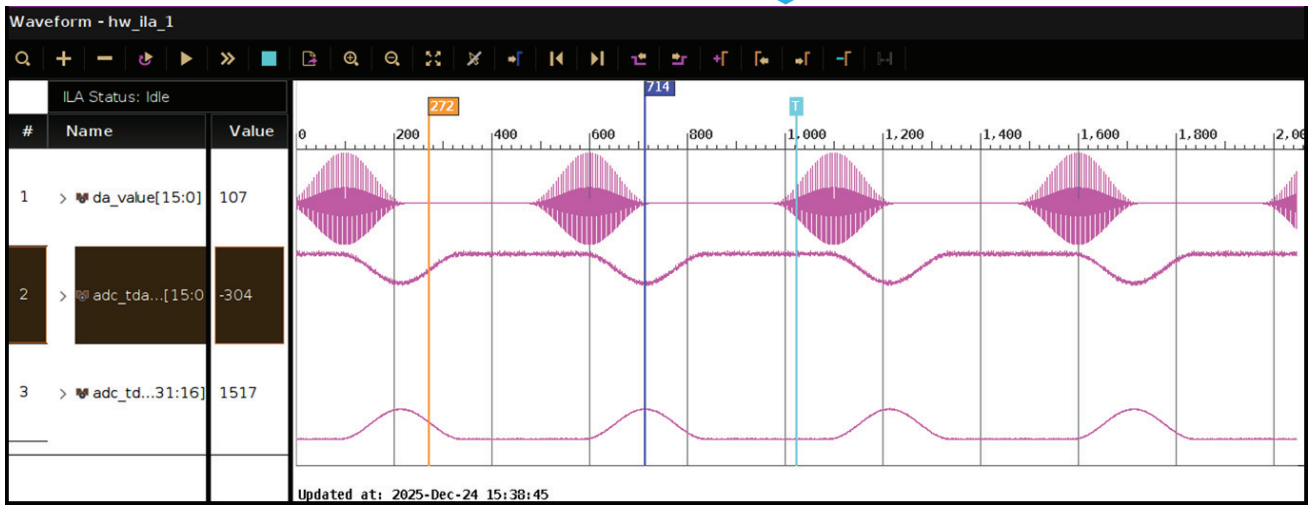
Procedure: Application with Embedded IOC



DSASettings.Attenuation = 10.0
DSASettings.DisableRTS = 1

RFDC Linux Driver Software Architecture Based on UIO



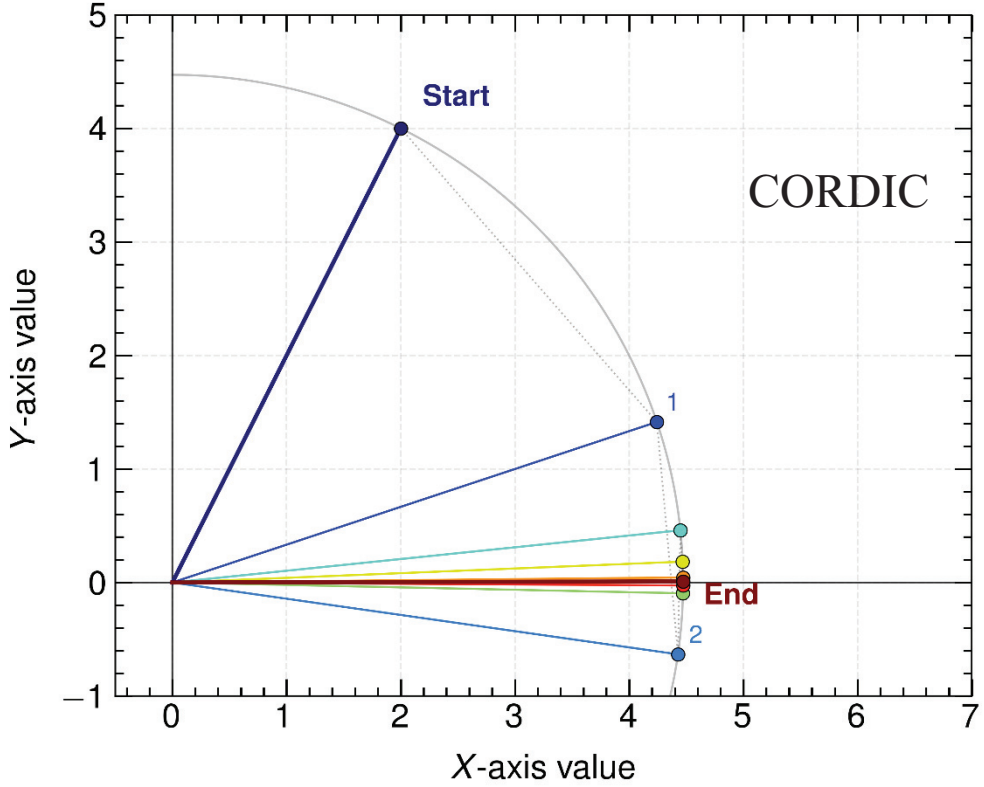


Experimental Validation of the DBCM Prototype

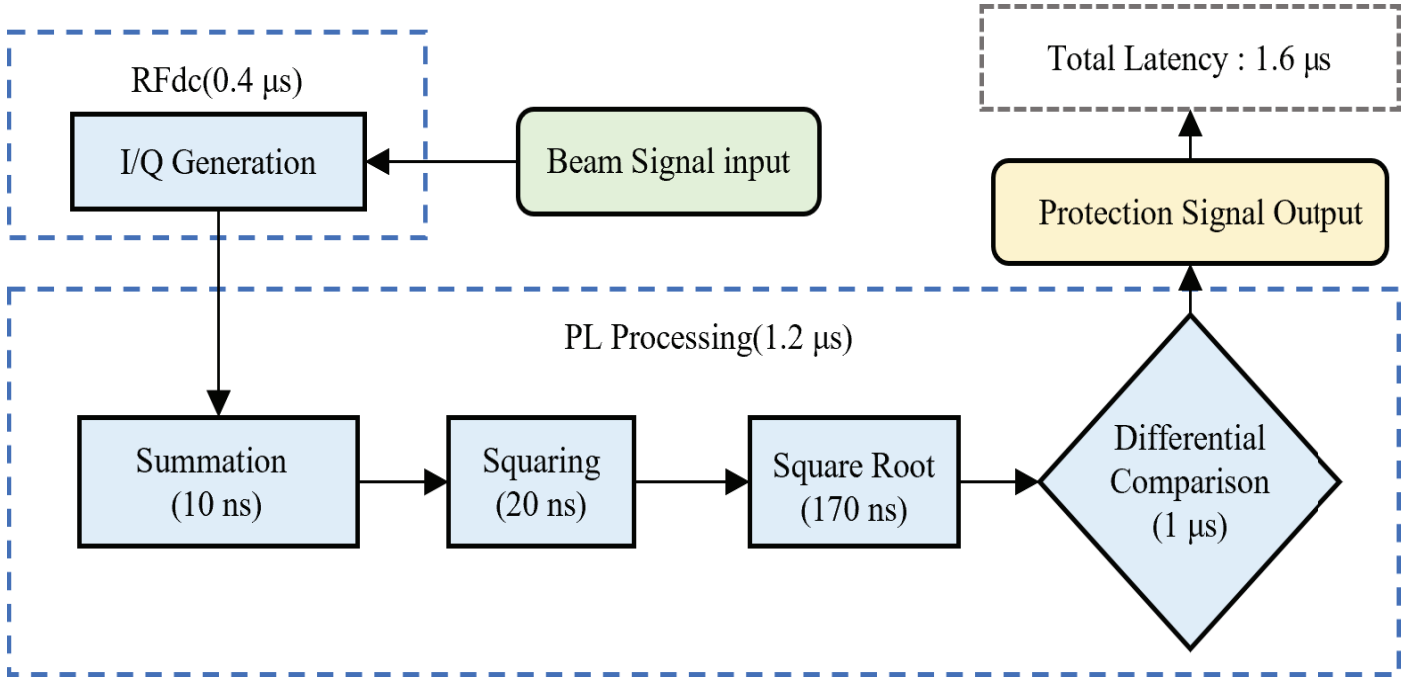
■ Design: Data Computation Module & Signal Processing

- Utilizes the CORDIC algorithm to perform complex calculations such as trigonometric functions, square roots, and magnitude calculations through simple shift-and-add operations.
- Particularly well-suited for the hardware parallel architecture and pipelined real-time processing of FPGAs.

CORDIC Vector Rotation Process



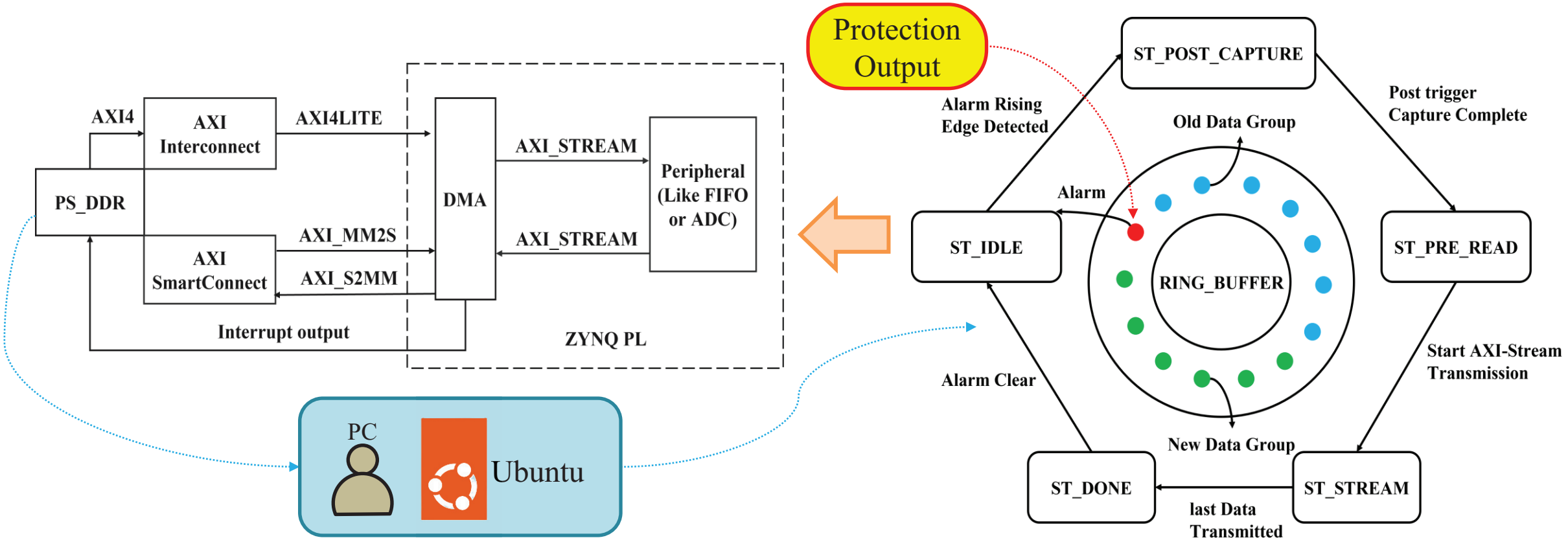
Comprehensive Analysis of Module Timing Paths



Experimental Validation of the DBCM Prototype

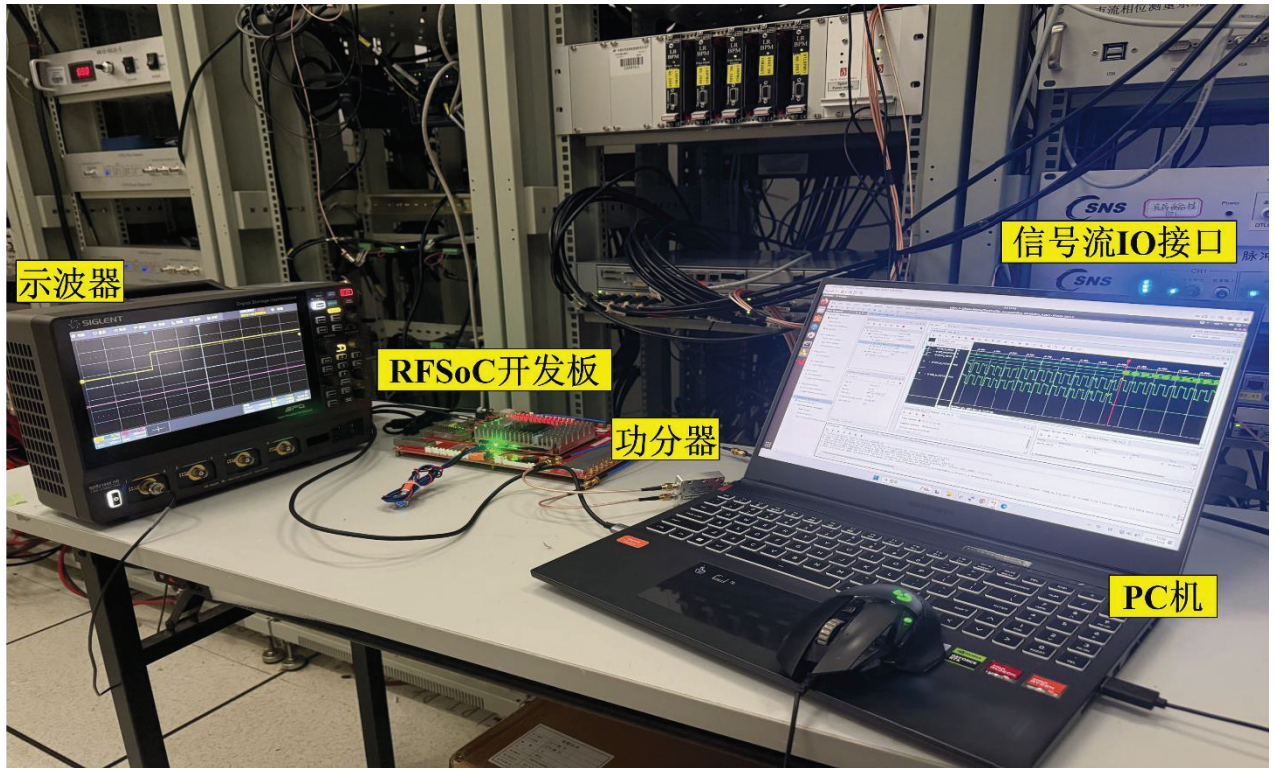
Design: Data Buffer Module Design

- A state machine then packs the data into an AXI4-Stream format that complies with the DMA transfer protocol.
- An asynchronous FIFO is utilized for clock domain crossing (CDC) synchronization.
- The data is written to the DDR4 memory on the PS side via the DMA controller and read by the host computer.

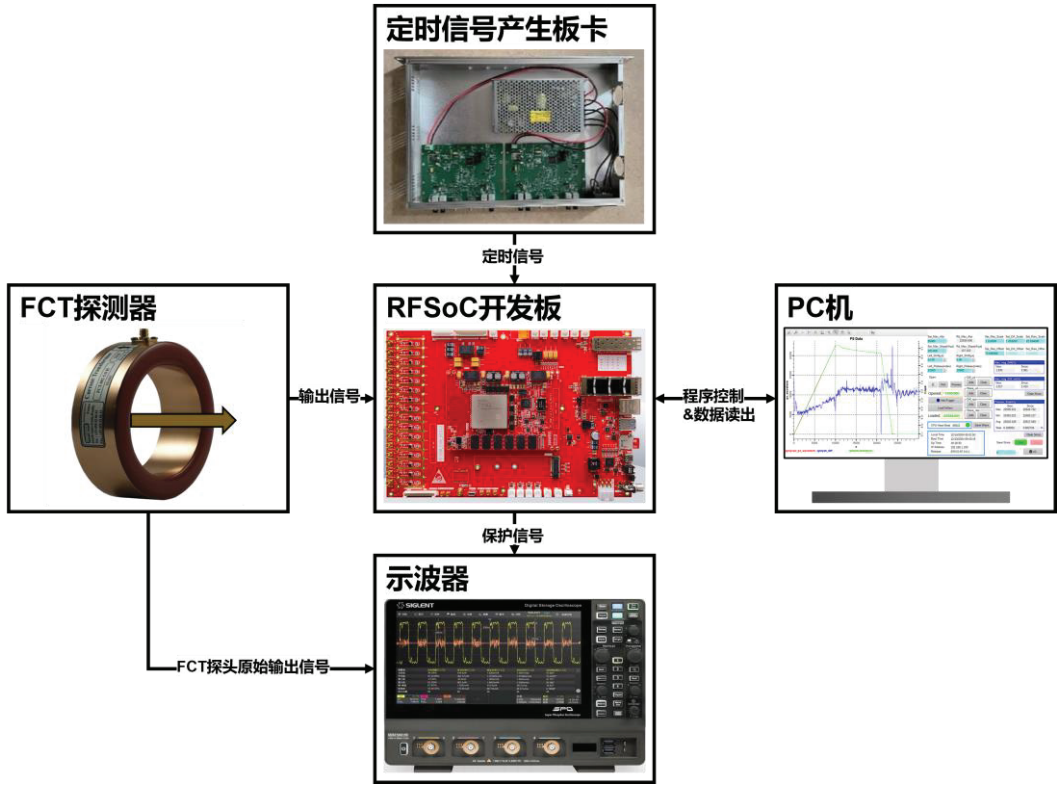


Experimental Validation of the DBCM Prototype

- **Test Setup:** Due to the availability of only a single FCT testing device, a power splitter was employed to divide the FCT output into two identical signals, which were then fed into the development board for dual-channel comparative processing.



Field Test Scenario

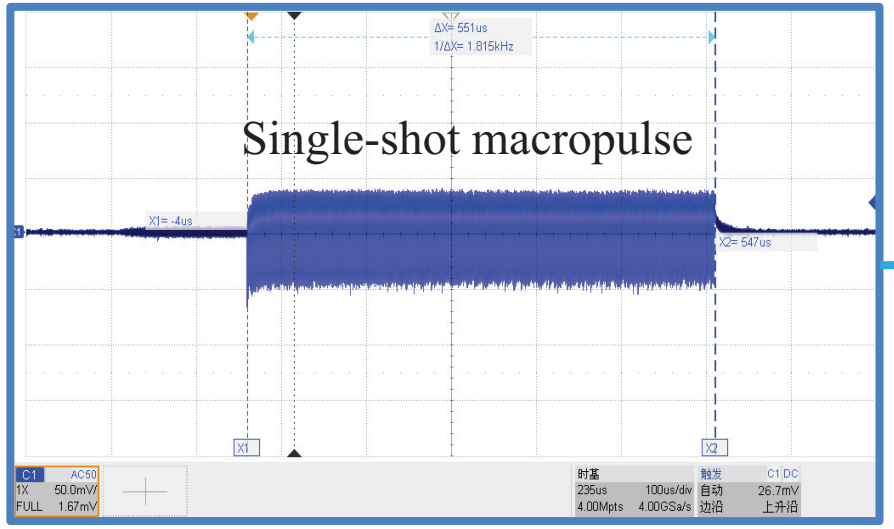


Equipment Connection Block Diagram

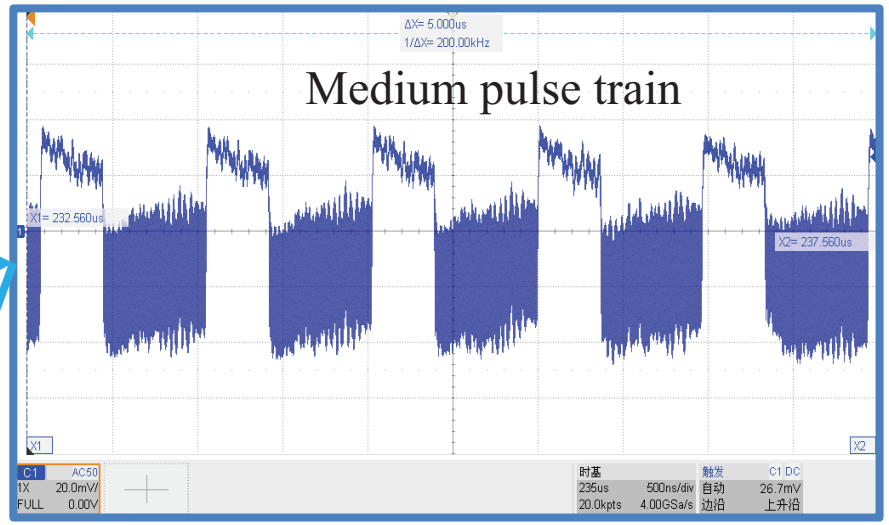
Experimental Validation of the DBCM Prototype

■ Performance under Normal Beam

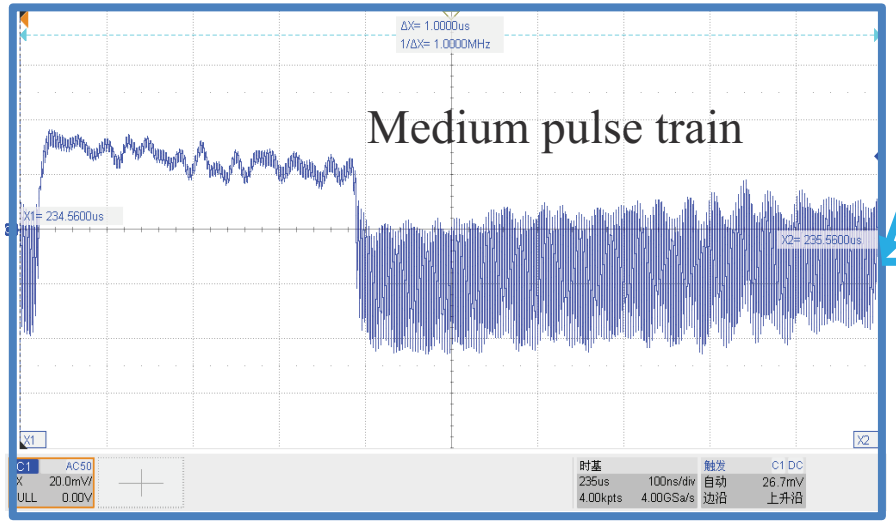
Substituting BCM with Online FCT for validation



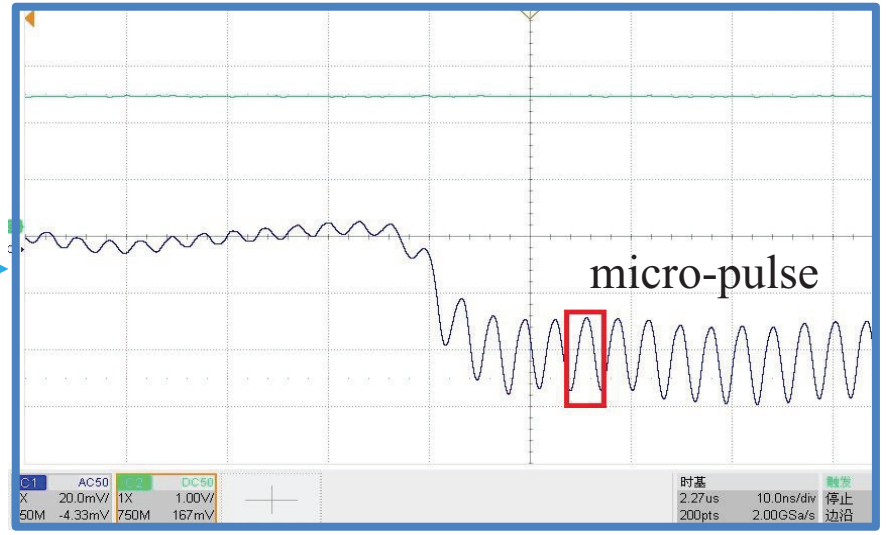
zoom in



zoom in



zoom in

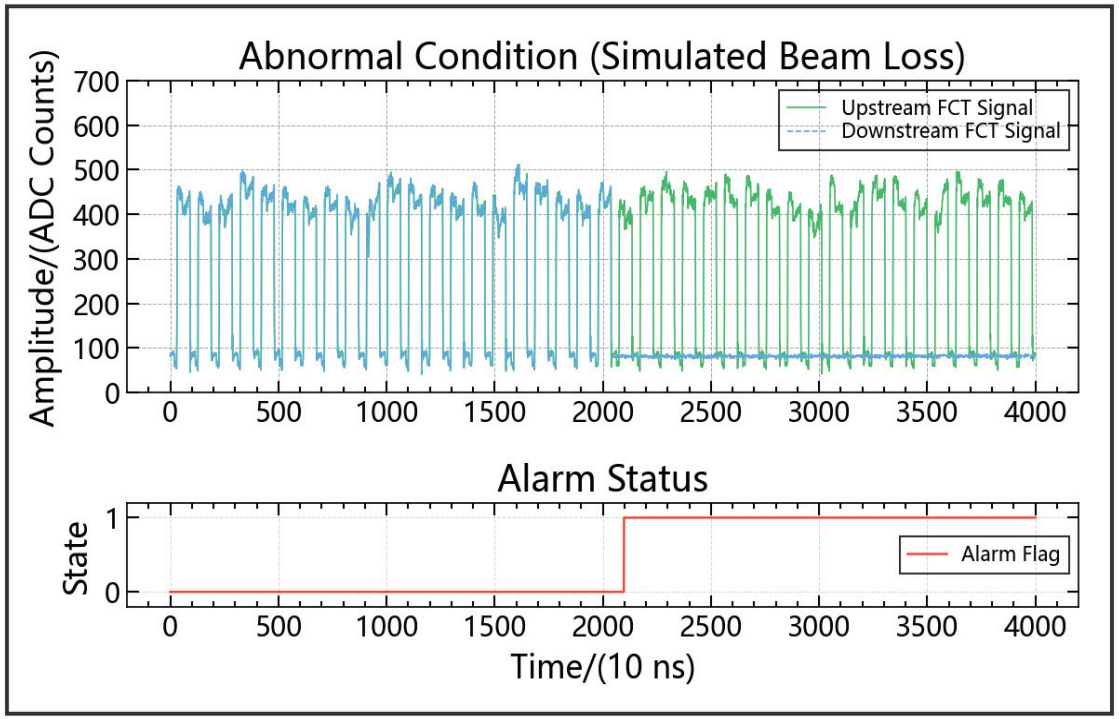


Experimental Validation of the DBCM Prototype

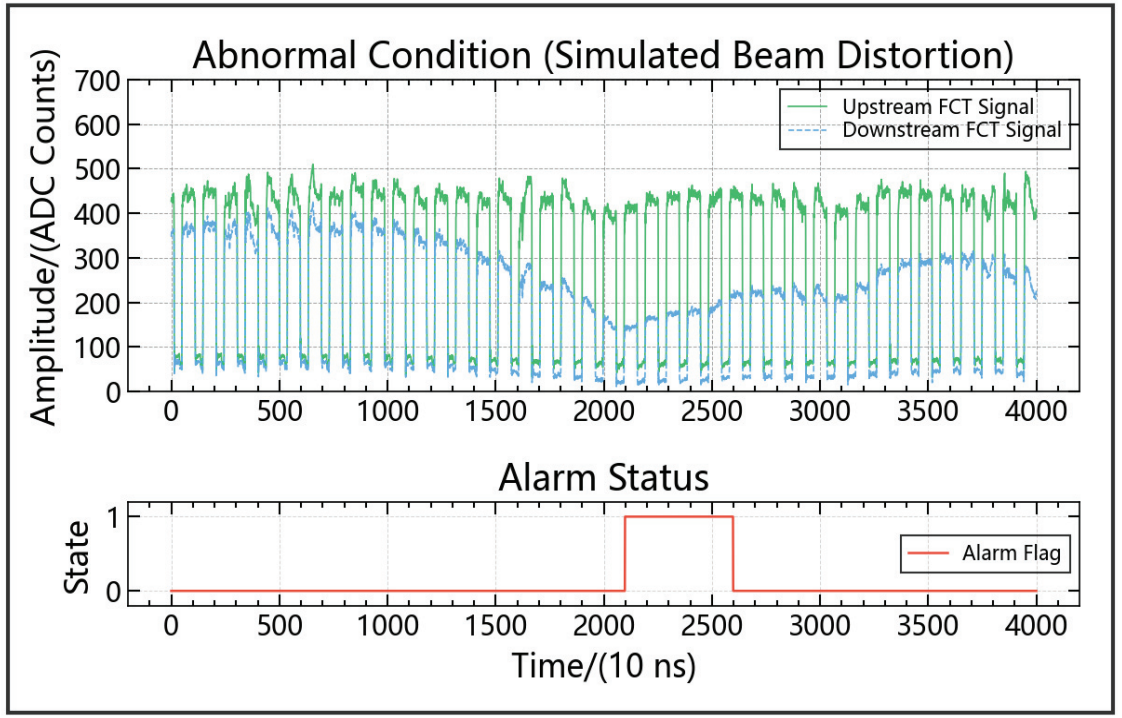
■ Validation under Abnormal Conditions (Simulated Beam Loss/Distortion)

➢ Under the normal beam mode, the waveforms of the two channels were consistent, and no alarm was triggered.

➢ When simulating two abnormal conditions, bunch loss and waveform distortion, the system immediately initiated a protection response once the signal difference exceeded the alarm threshold.



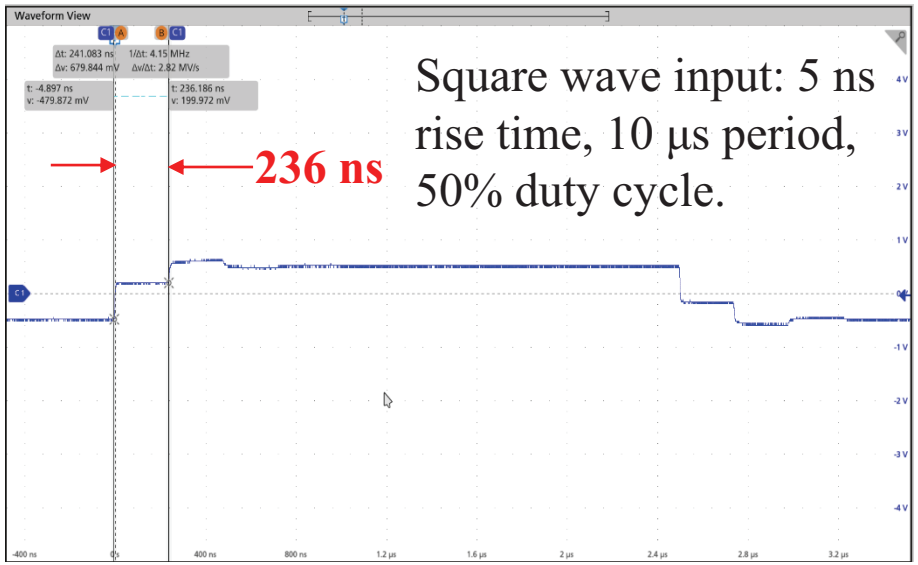
Simulating downstream beam loss

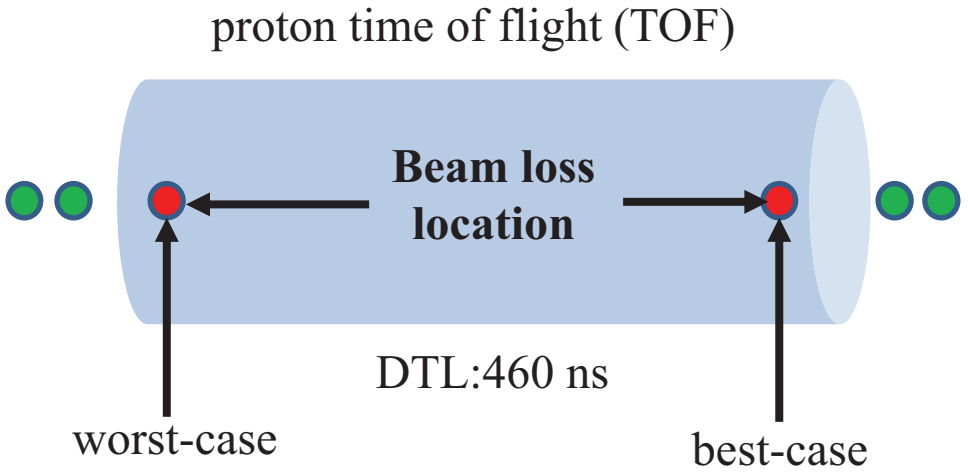


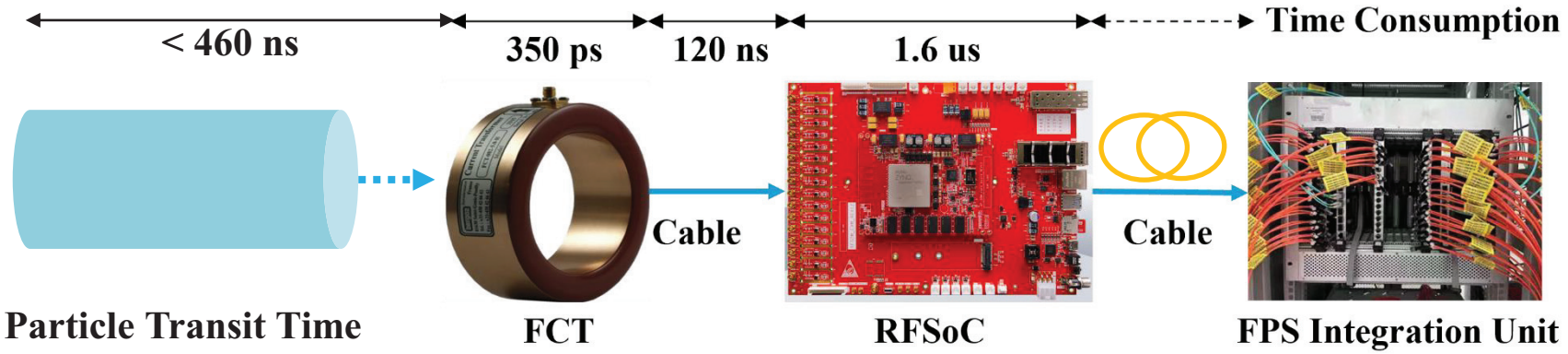
Simulating downstream beam waveform distortion

Experimental Validation of the DBCM Prototype

- **System Latency Evaluation:** The DBCM logic takes ~1 μs. Including ~2.5 μs of cable delay and ~1.5 μs of beam propagation time (TOF), the overall system latency is approximately 5 μs.





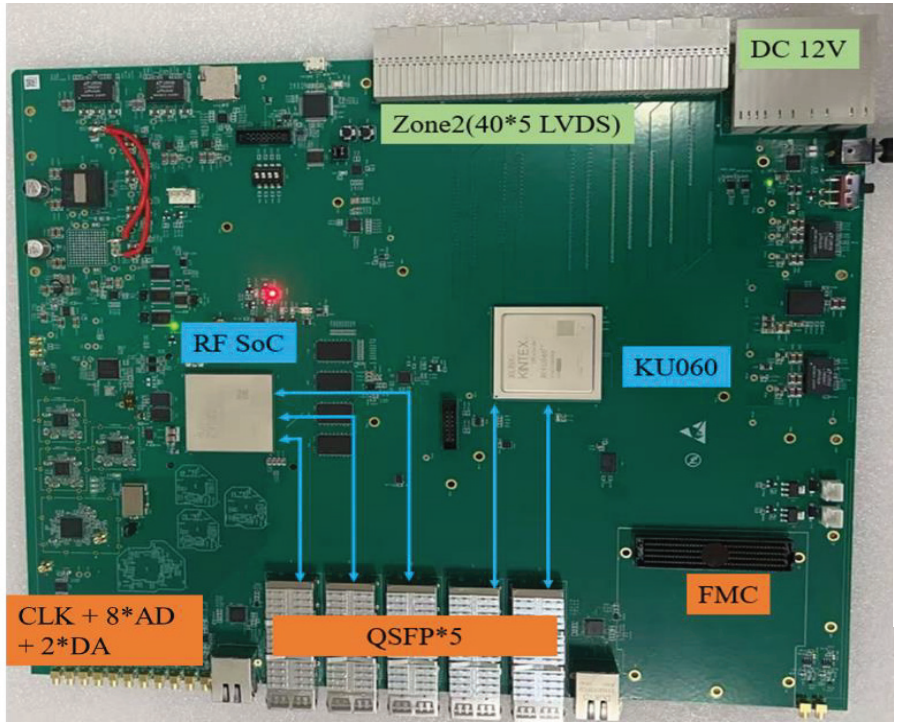


Estimated overall system latency: 5 μs, meeting the protection requirements for future superconducting cavities.

Future Work

Active Protection Mechanism:

From "Triggering" to "Prediction"



- Real-time processing: Sliding average filtering & baseline subtraction
- Edge AI deployment: 1D-CNNs / Autoencoders via hls4ml
- Pipelined inference: Triggered at fixed beam-cycle intervals.

Built on a self-developed advanced hardware data processing platform featuring "RF SoC + KU060".

Summary

- Adopt ATCA architecture based on a customized backplane and self-developed front boards as the solution.
- Using one main logic board (Embedded IOC) and four types of interface boards to cover most applications.
- Combining DBCM with AI in the linear superconducting section is expected to further enhance the performance.
- Integrating BLM and the FPS into a unified platform is challenging, and the real-time data with high-precision timestamps is worthwhile to explore (EVR function).

Thank you for your attention!