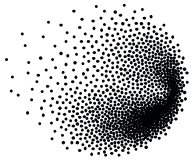

PSI Center for Accelerator Science and Engineering

Real-Time Direct Sampling Bunch-by-Bunch Arrival Time Measurement on RF Systems-on-Chip for Multi-Bunch Feedbacks (MBFBs)

Boris Keil, Pedro Baeta, David Madlener

15th International Beam Instrumentation Conference, Whistler BC, Canada, August 30 - September 3, 2026

Legacy Analog Mixer MBFB @ SLS 1.0: Principle and Limitations

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Traditional longitudinal MBFB: analog down-conversion

Concept:

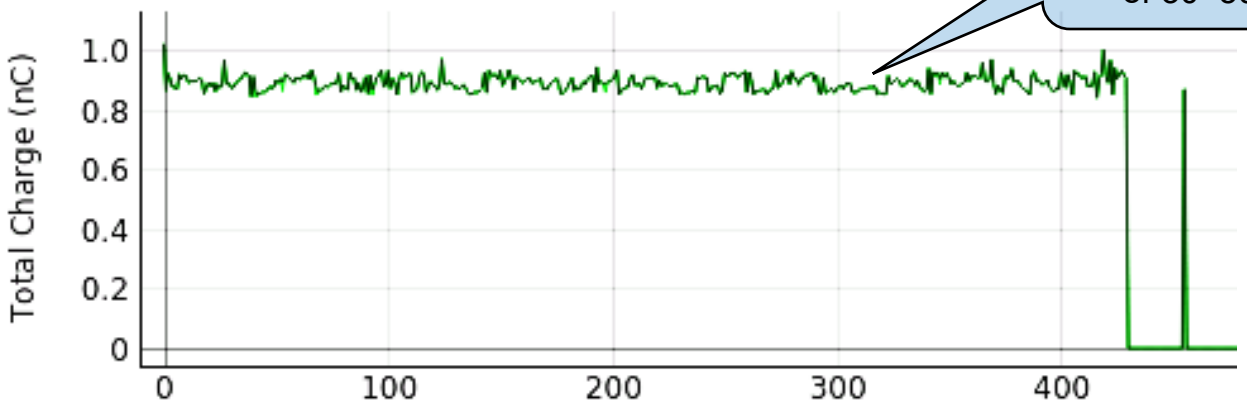
- BPM-button sum signal → 1.5 GHz band-pass → mixer
- Mixer driven by a 1.5 GHz local oscillator (LO) locked to the machine RF
- LO phase tuned so the nominal bunch arrival time gives zero mixer output

Limitations:

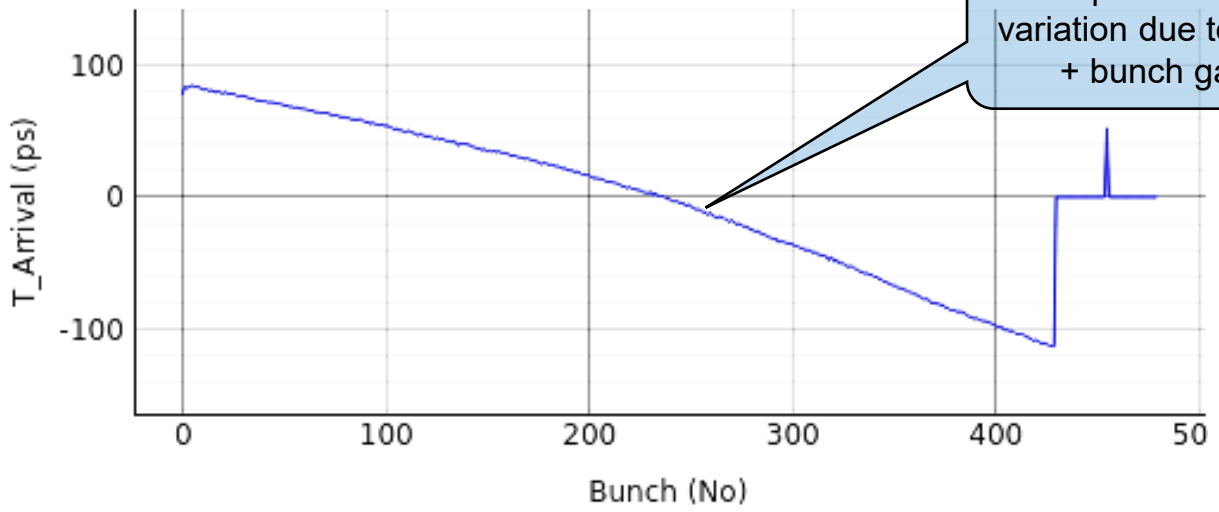
- Mixer output contains both bunch charge Q and timing error Δt
  - Bunch-to-bunch charge variation therefore changes the apparent feedback gain
- Linear in arrival time only near the tuned zero crossing
  - Larger timing deviations become nonlinear and can even reverse the gain sign
  - At SLS: passive 3HC + bunch gap produces ~200 ps arrival-time variation across the train

Legacy Analog Mixer MBFB @ SLS 1.0: Bunch No. Dependent Gain

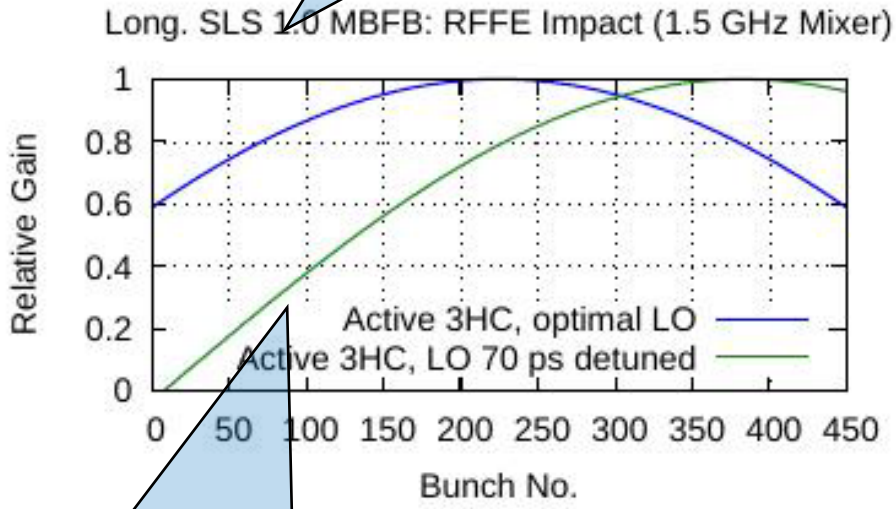
Typically 430–450 of 480 bunches filled; gap of 30–50 bunches



~200 ps arrival-time variation due to 3HC + bunch gap

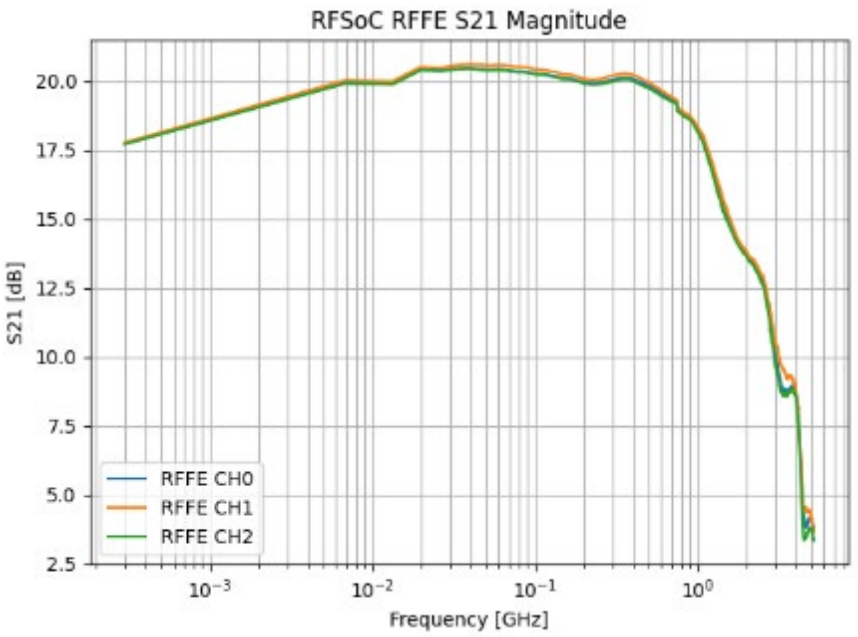


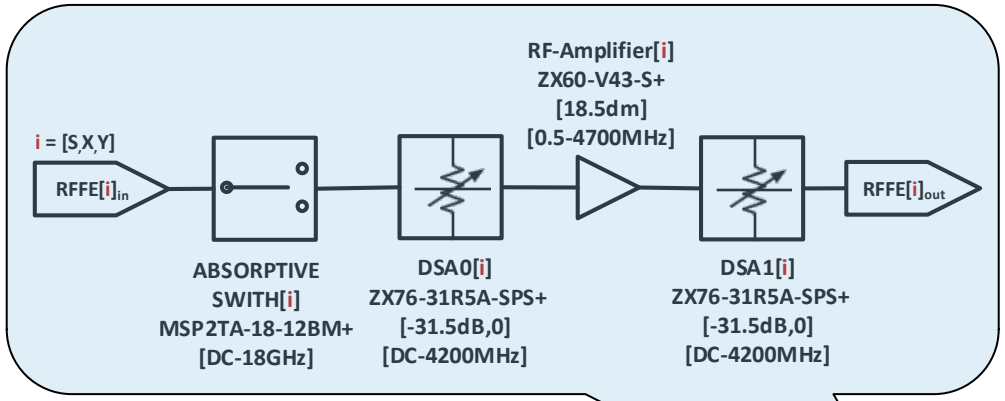
Result: SLS 1.0 RFFE makes MBFB gain depend on bunch number / arrival time

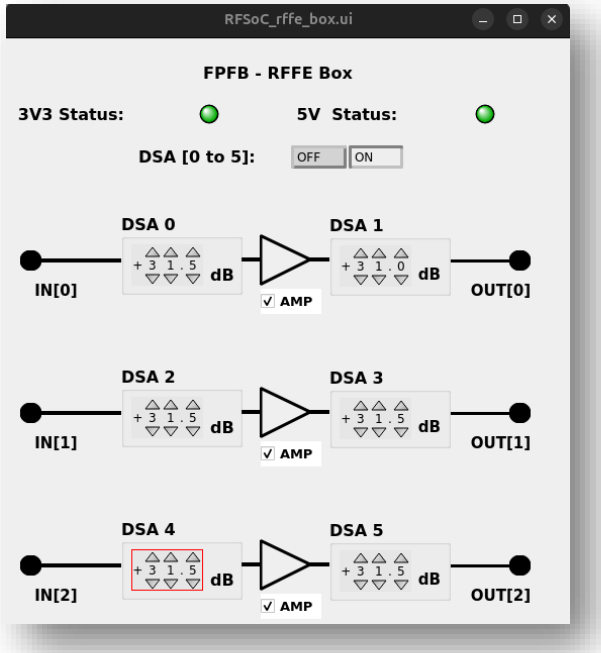


1.5 GHz LO phase must be tuned carefully; detuning can cause much larger gain variation or even negative gain

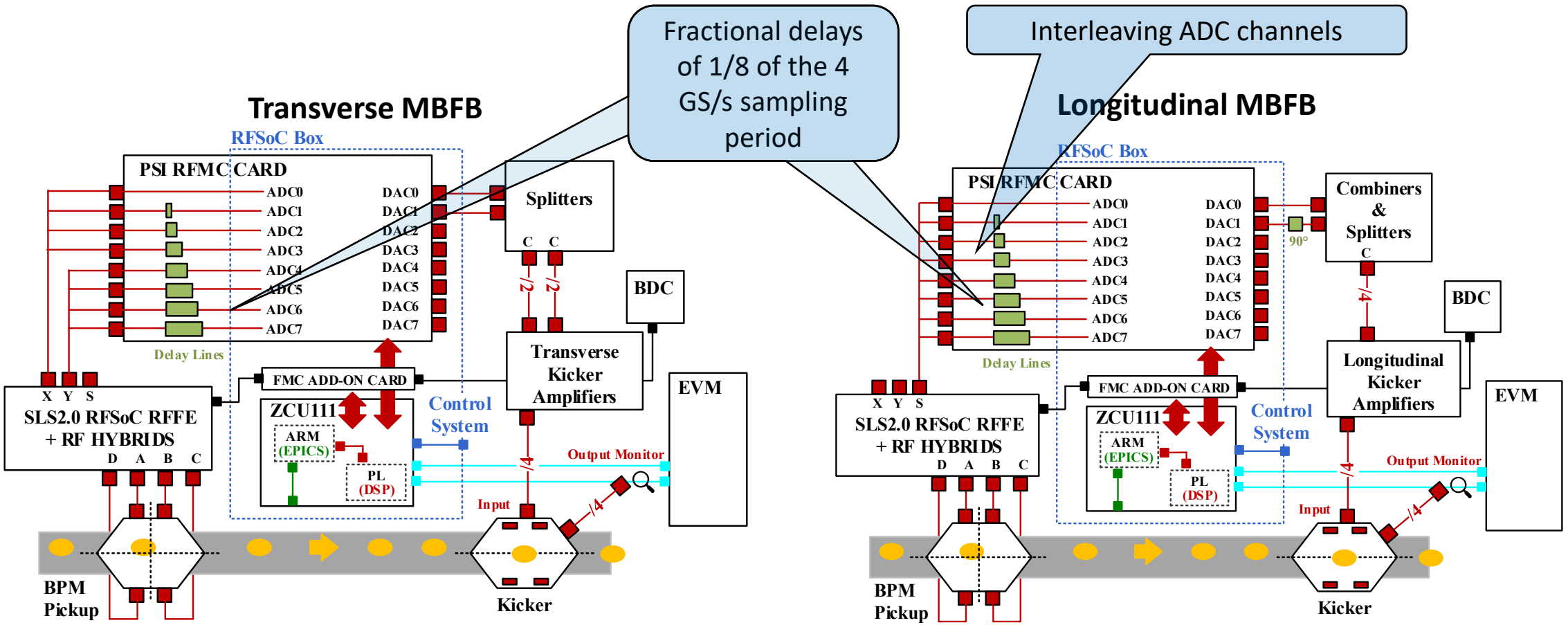
Direct Sampling @ SLS 2.0: Simple 3-Channel RFFE, No Mixer



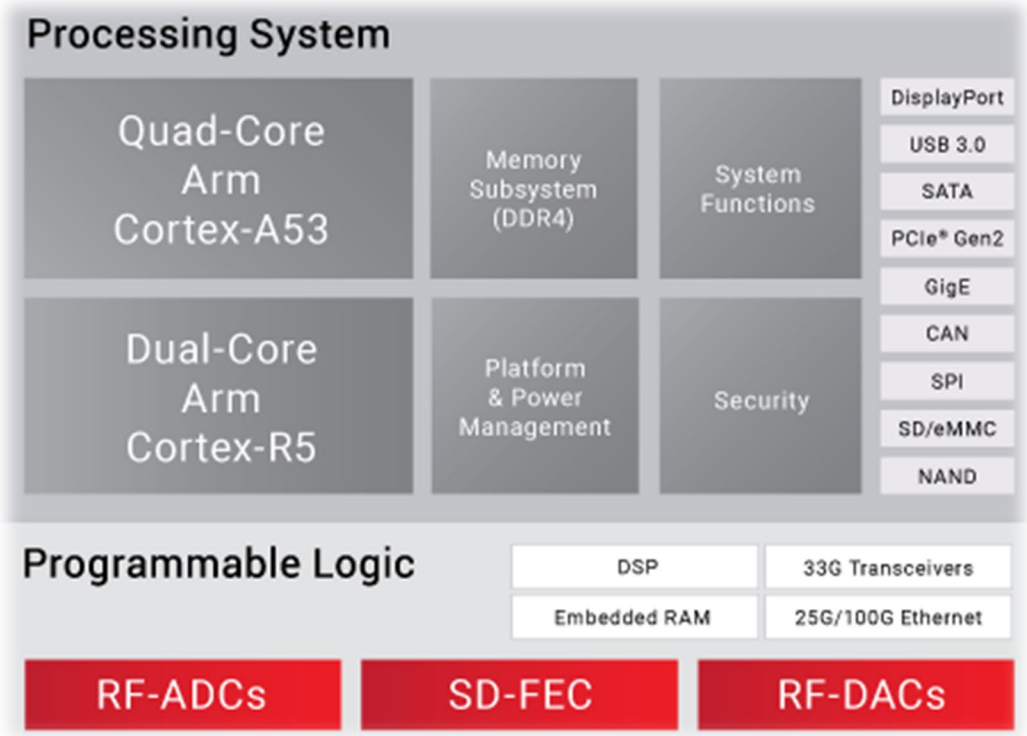




Direct Sampling & Kicker Driving @ SLS 2.0: Hardware



Direct Sampling @ SLS 2.0: AMD RFSoC Gen 1 for MBFB/FPFB



Zynq® UltraScale+™ RFSoC Gen 1 [3]

Integrates:

- Multiple CPUs
- Large FPGA fabric
- GHz-range ADCs and DACs
- Memory and high-speed communication interfaces

Low ADC-to-DAC latency

- **8 ADCs (12 bit, up to 4.0 GSample/s): ~46–101 ns**
- 8 DACs (14 bit, up to 6.5 GSample/s): ~24–116 ns
- ADC + DAC loop-back latency: ~70–217 ns
  - Example: 348 sample clocks = 87 ns at 4 GSample/s
- Stable and reproducible after power cycle*
  - ***Multi-tile synchronization (MTS) required.**

Stable temporal sample alignment among ADCs and DACs

- Multi-tile synchronization (MTS) mode

SLS 2.0: Direct sampling of the RF BPM sum signal

Concept:

- **BPM-button sum signal sampled directly at 32 GSample/s with the RFSoC**
  - 8 ADC channels × 4 GSample/s interleaved using splitters and tuned delay lines
- RFSoC FPGA processes the full 32 GSample/s stream continuously with low latency

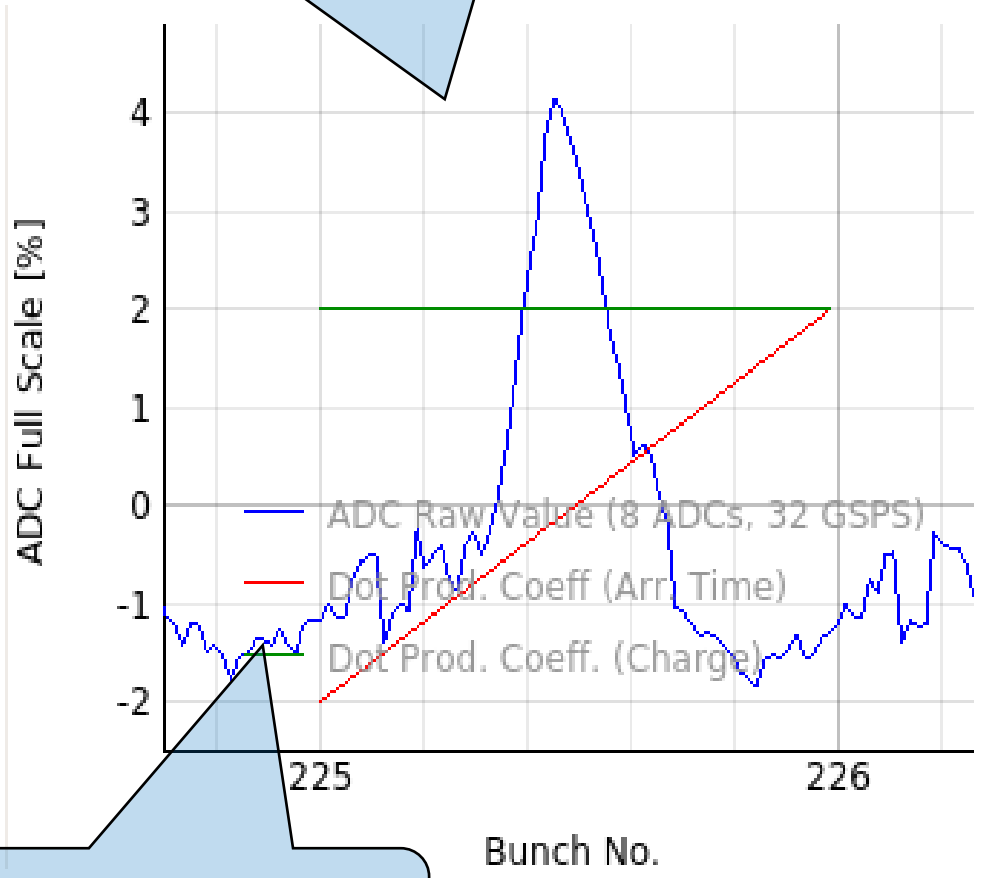
Benefits:

- **Digital dot products of ADC data (64 samples per bunch, negative values cut off)** and coefficient vectors (EPICS programmable) **measure Q and Q·Δt; division yields arrival time Δt** independent of bunch charge
- Much wider linear timing range; no phase-tuned analog LO required

Direct Sampling @ SLS 2.0 MBFB: Digital Dot-Product Method

SLS 1.0: analog mixer multiplies the beam signal by 1.5 GHz sine/cosine. The output is proportional to Q or Q·Δt only near the tuned phase.

SLS 2.0: sample directly at 32 GSample/s. Constant weights → Q; linear weights → Q·Δt; divide the two → arrival time Δt.

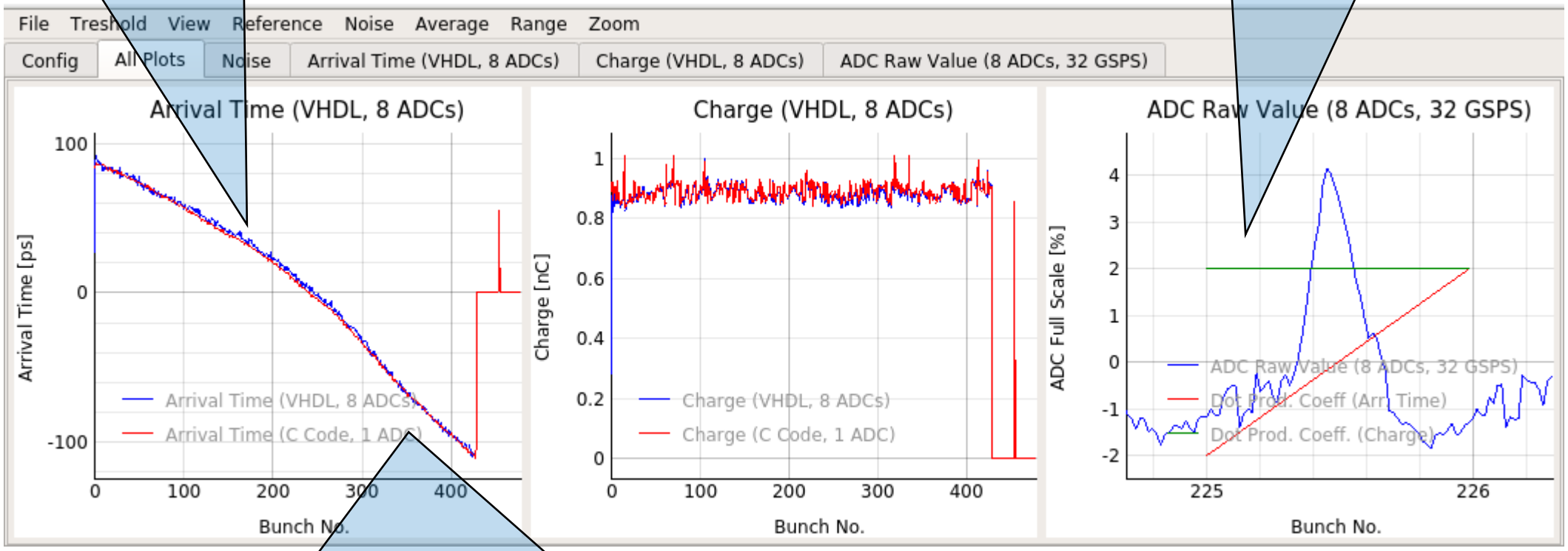


SLS 2.0: Negative ADC values set to 0 before dot product calculation, leaving only short positive peak that carries arrival time information

Beam Test @ SLS 2.0: New MBFB Method (FPGA) vs. FPFB (CPU)

Reference Filling pattern feedback (FPFB, red curve): 1 ADC, equivalent-time sampling over 16 turns, C code on ARM CPU (~100 ms). Accurate, but too slow for MBFB.

64 dot-product coefficients for Q (green) and Q·Δt (red) can be adjusted live via EPICS

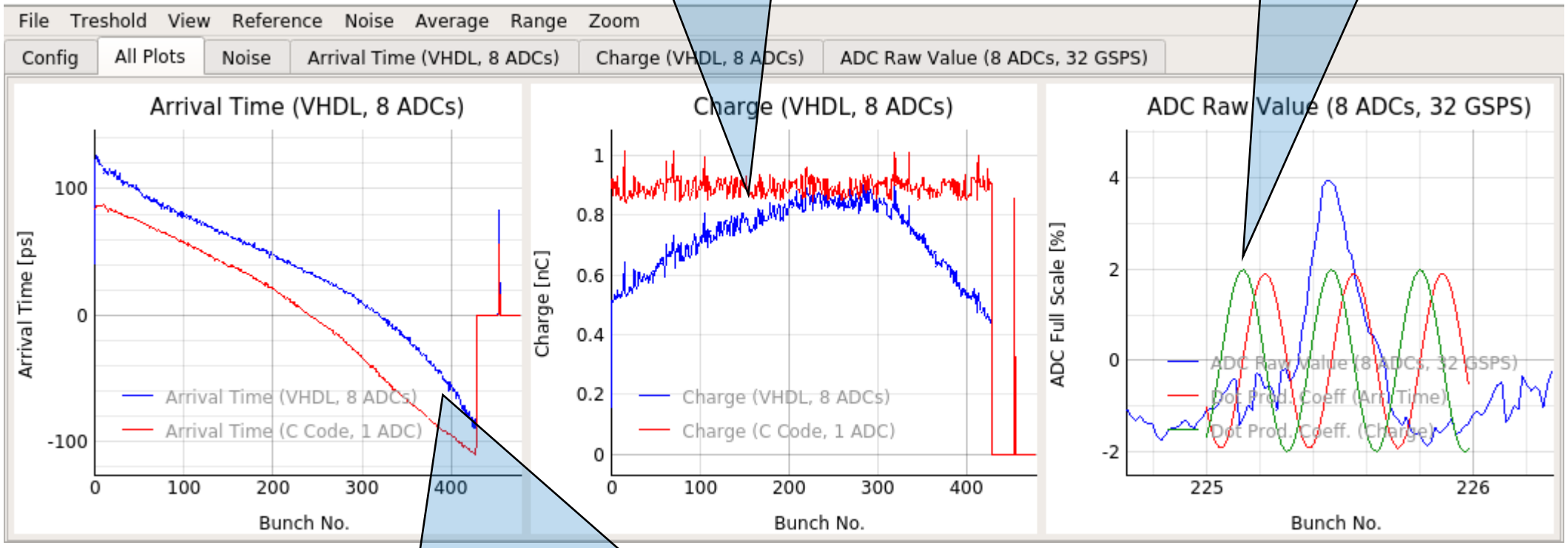


New MBFB FPGA implementation (blue curve): continuous 32 GSample/s stream, 312 ns pipeline latency. Result ≈ FPFB reference (BPM-based version = default, we also have photon-based backup, see poster by Daniele Felici, TUP037)

Beam Test @ SLS 2.0: MBFB FPGA Emulating Analog SLS 1.0 Mixer

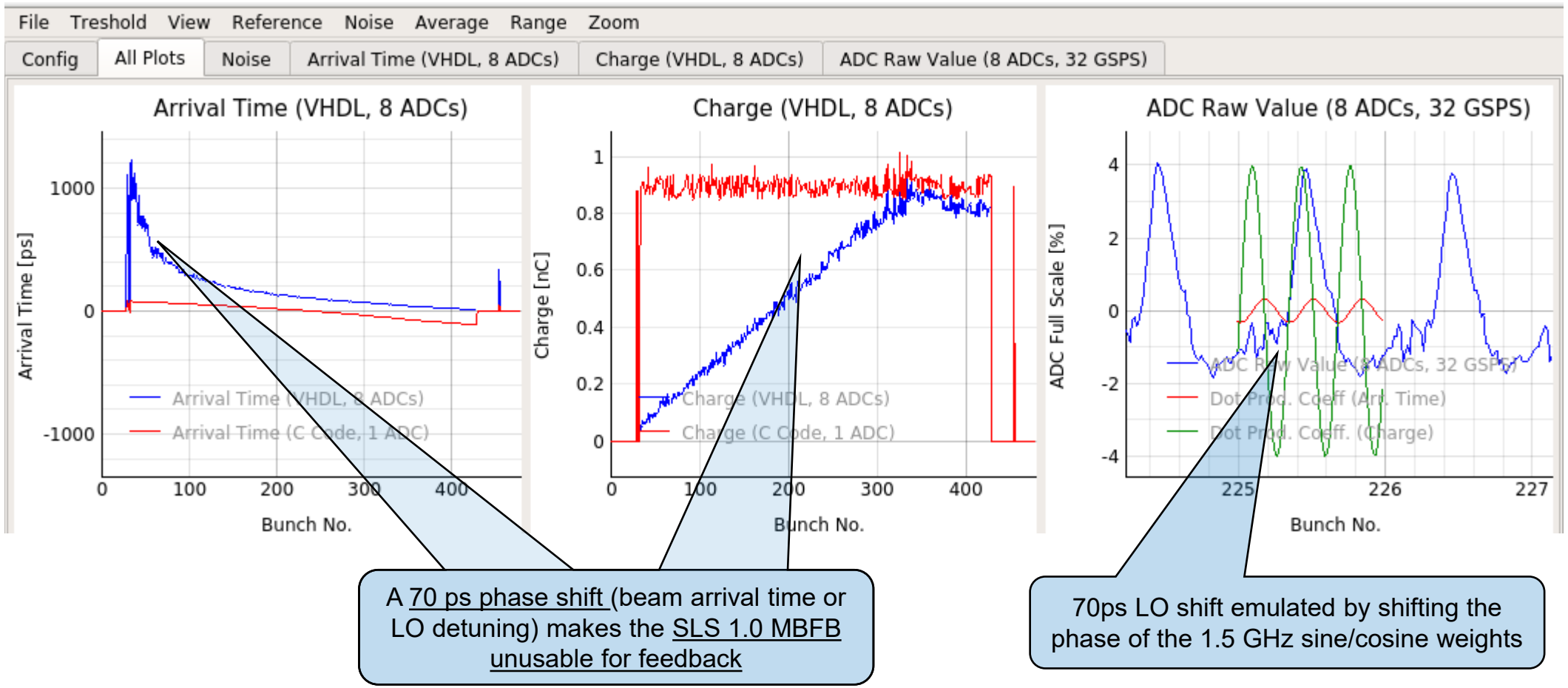
Charge (blue) now varies strongly with bunch number, reproducing the legacy gain error. Red = FPFB reference.

For validation, program 1.5 GHz sine/cosine weights to emulate the SLS 1.0 analog mixer



Arrival time of SLS 1.0 MBFB (and derivative = relevant for feedback) remains usable only when the equivalent LO phase is well tuned

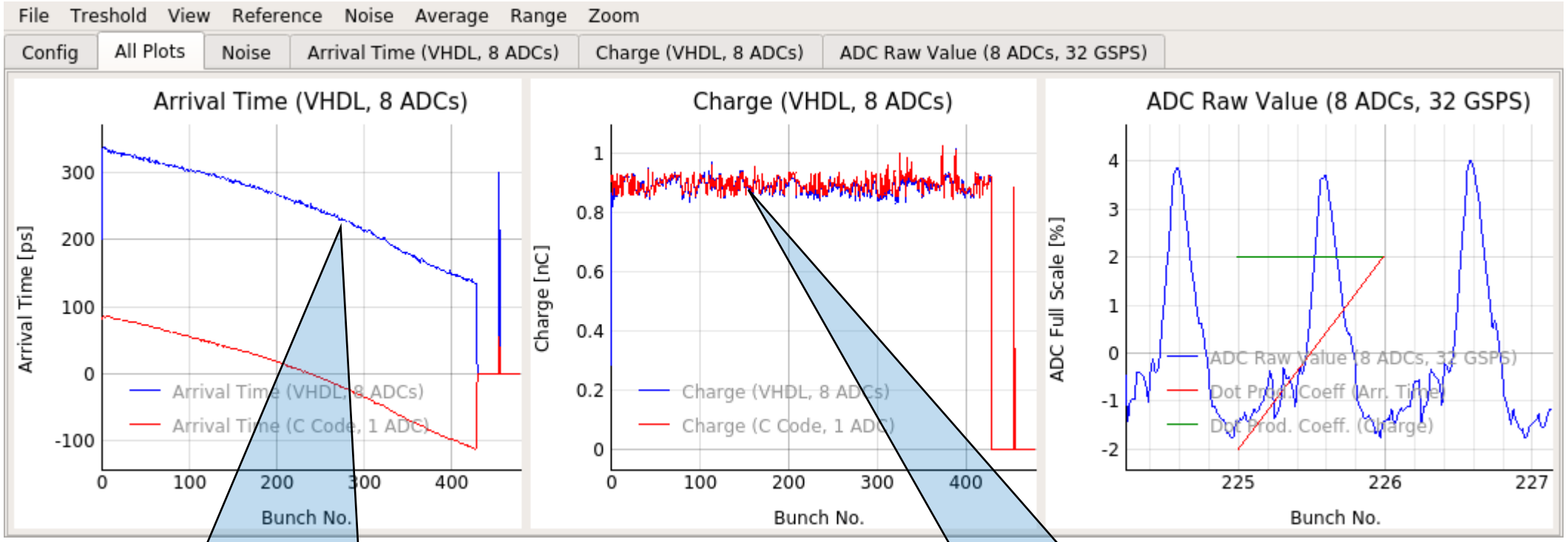
Beam Test @ SLS 2.0: 70 ps Phase Shift Breaks the Legacy Method



A 70 ps phase shift (beam arrival time or LO detuning) makes the SLS 1.0 MBFB unusable for feedback

70ps LO shift emulated by shifting the phase of the 1.5 GHz sine/cosine weights

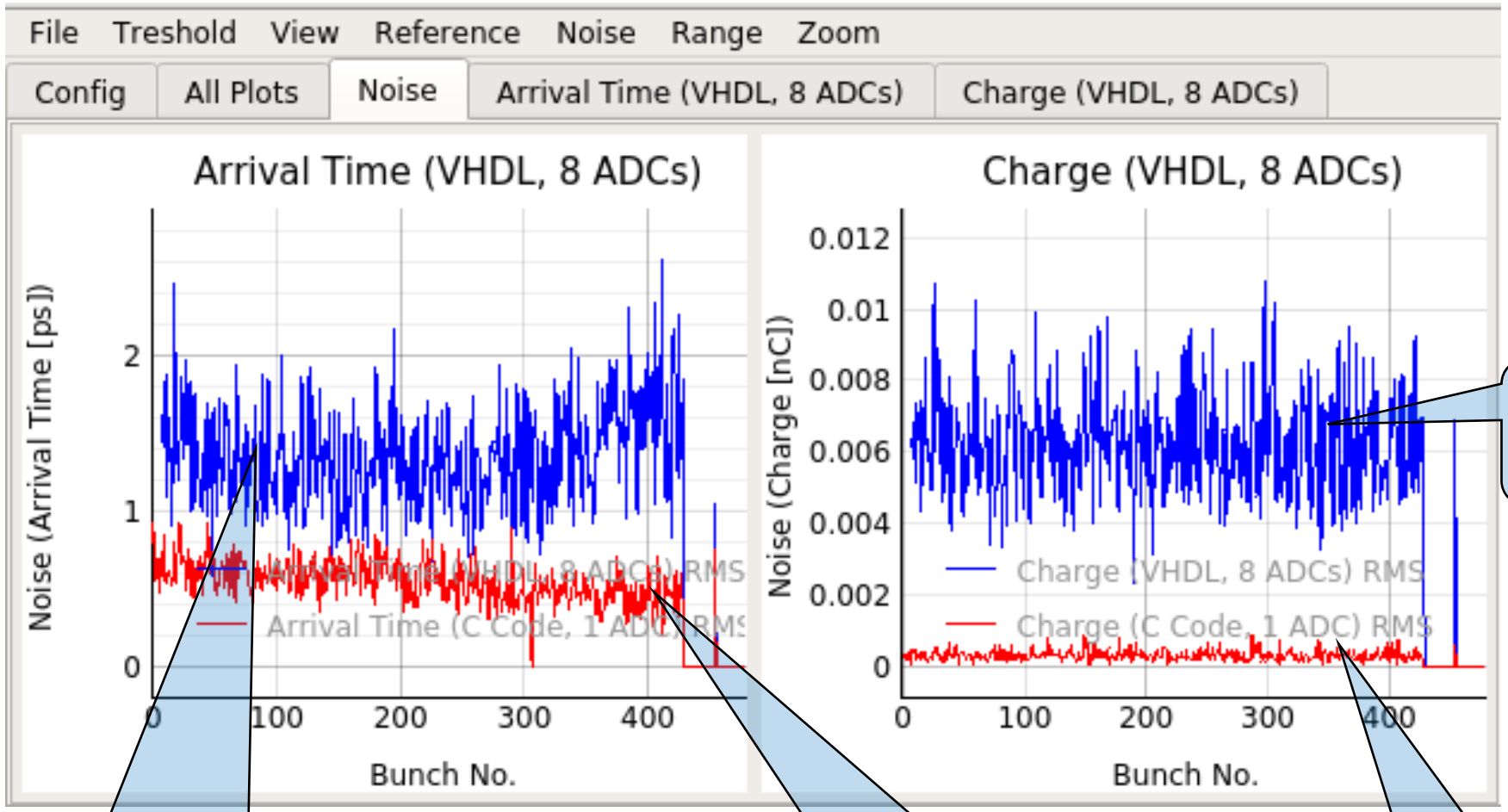
Beam Test: Direct Sampling Stays Linear for a 250 ps Shift



New SLS 2.0 MBFB: a +250 ps sampling shift produces an approximately common +250 ps offset across the bunch train → zero impact on feedback

Charge measurement also unchanged by the 250 ps shift: Still agrees with the FPFB reference

Beam Test: Direct Sampling MBFB Noise (FPGA) vs. FPFB (CPU)



Blue: MBFB (FPGA), 8 ADCs, **1 turn, no averaging**.

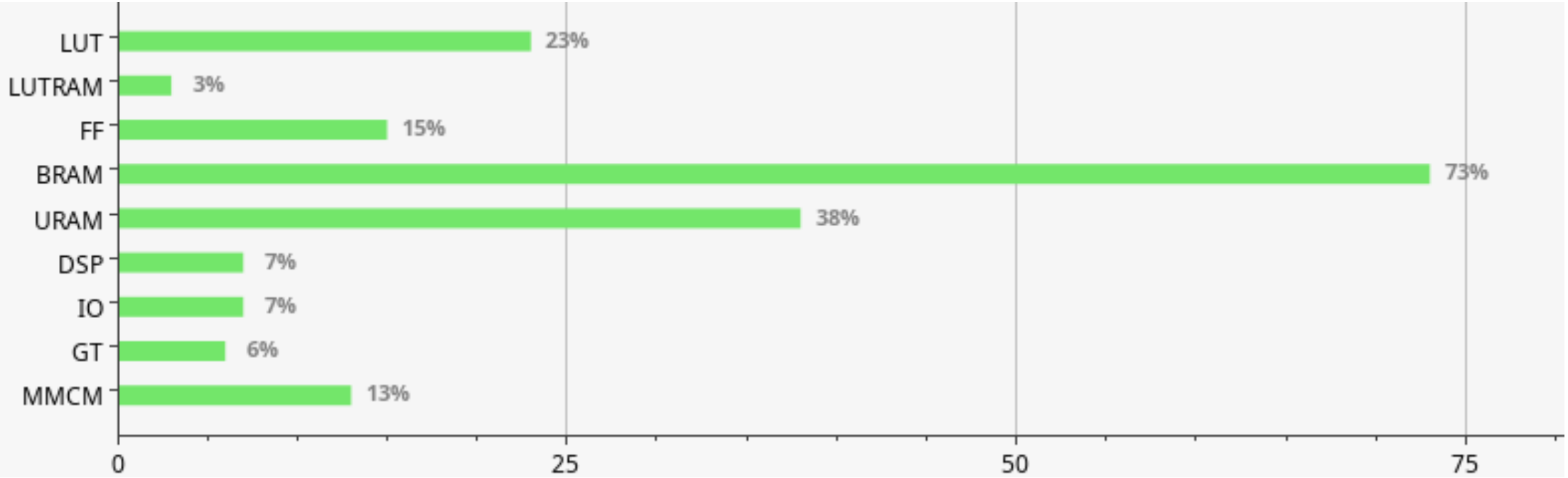
Blue: MBFB FPGA implementation, 1 turn only, 8 ADCs interleaved, only 4% of ADC range used, can be improved.

Red: FPFB Algorithm in CPU, 1 ADC, 16 turns fractional clock sampling.

Red: FPFB (CPU), 1 ADC, 16 turns, **10x averaging (160 turns).**

FPGA Resource Usage: Ample Logic Margin

- Current firmware includes ADC acquisition, charge/arrival-time dot products, on-chip buffers, DAC function generator, event receiver, and EPICS interface; closed MBFB loop with direct kicker drive is not yet implemented.
- BRAM/URAM usage is intentionally high for test buffers. Moving long buffers to external DRAM will free most of this memory; logic/DSP utilization is already low (LUT 23%, FF 15%, DSP 7%).



RFSoC FPGA Resource Usage [%]

Additional FPGA Latency

Block	Latency
ADC CDC and 128→256 packing	13 processing clocks
Pulse align	1 clock
ADC broadcaster 1	1 clock
ADC broadcaster 2	1 clock
8-ADC, 2-window interleave	1 clock
Dot product	7 clocks
Dot-product 1-to-2 broadcaster	1 clock
Division V2	53 clocks
Total	**78 clocks**

O.K. for SLS 2 (960ns revolution time), could be reduced for smaller rings

312 ns (250 MHz processing clock)

Outlook: Direct RFSoC Drive of the Longitudinal Kicker (Today)

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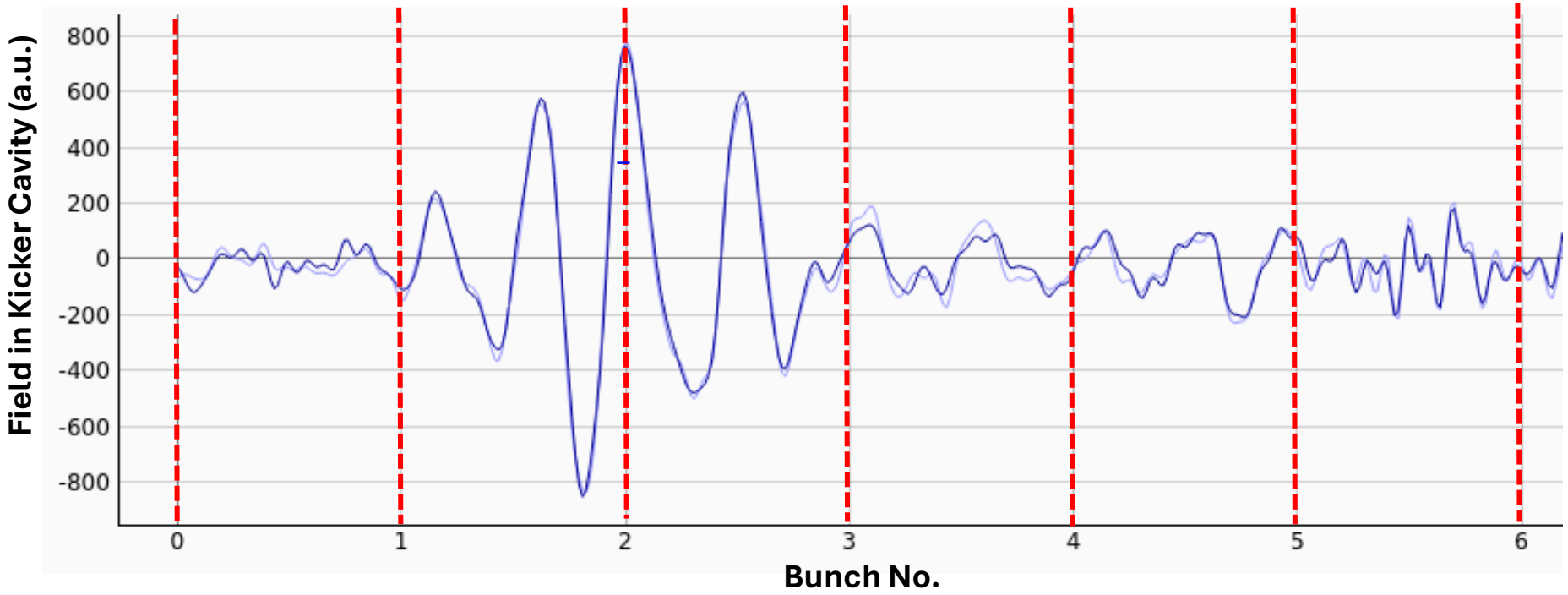
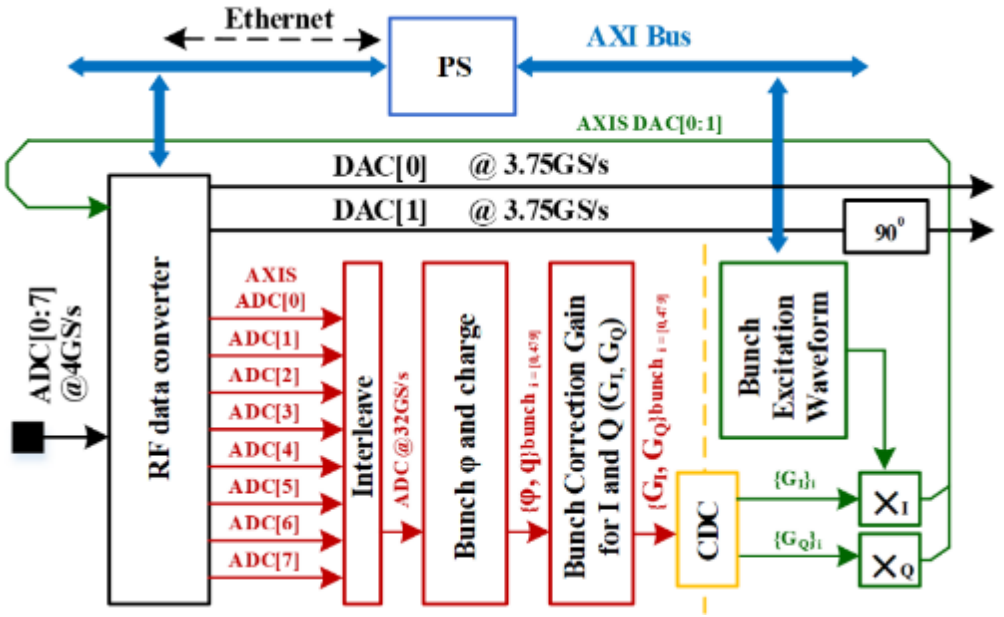
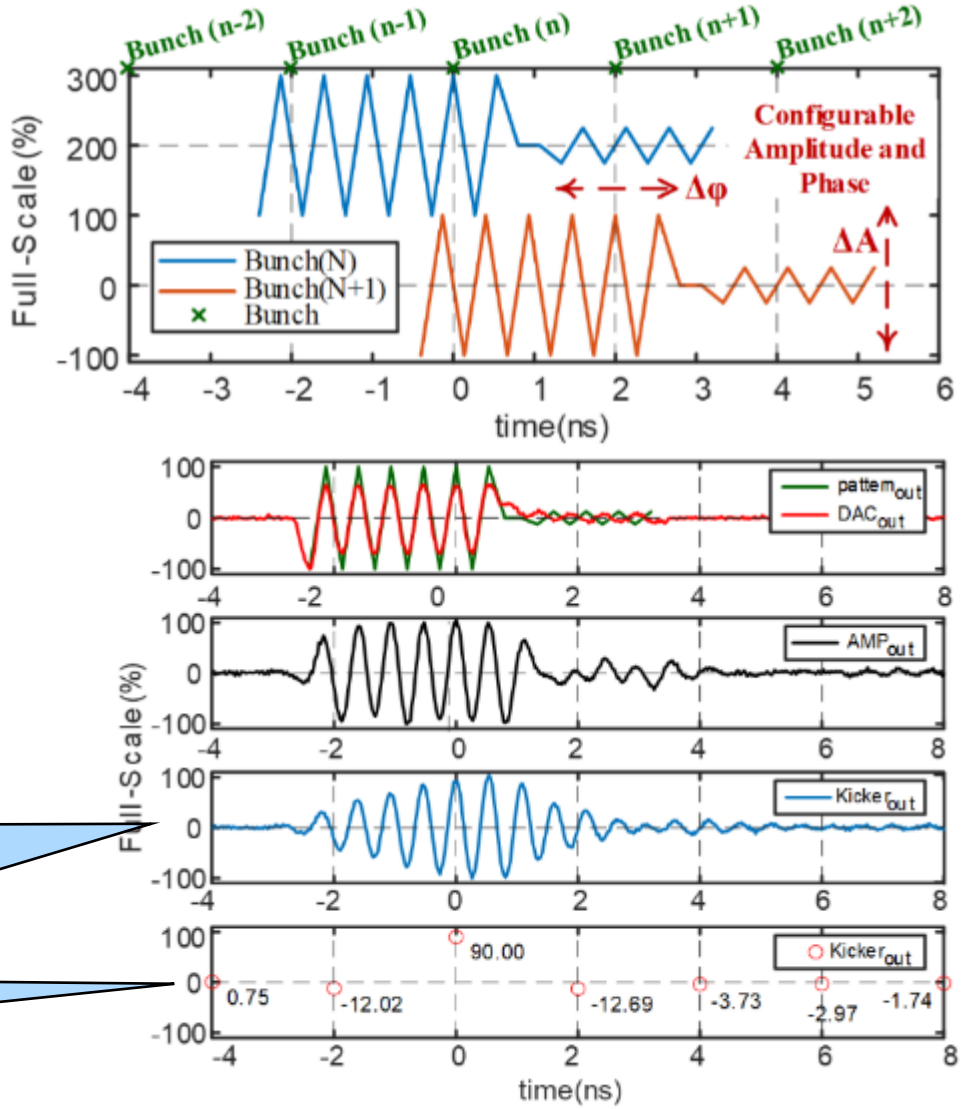
- SLS 1.0 longitudinal MBFB used an analog 1.375 GHz upconverter driven by a 500 MSample/s, 8-bit DAC — another source of bunch-dependent gain.
- SLS 2.0 goal: **drive longitudinal kicker power amplifier directly with 4 GSample/s RFSoC DACs**.
- **Plot: SLS 2.0 kicker-cavity field** for an optimized **2 ns-long, 4 GSample/s DAC waveform**; field measured with the 32 8GSample/s interleaved RFSoC ADCs.
- Strong kick at the target bunch, small kicks at neighboring bunches → suitable for feedback. Further crosstalk reduction is possible with FIR predistortion, a longer waveform, or I/Q DAC combination.



Outlook: Direct RFSoC Drive of the Longit. Kicker (1st Try Year 2024)





1st Try 2024: We used **a longer 3.75 GSPS DAC waveform**, so far only using RFSoC as function generator to check feasibility. Closing feedback loop at 3.75 GSPS feasible, but lot of effort (2 clock domains) → will **now use 4 GSPS** instead (DAC waveform less intuitive, but **firmware much easier**)

RFSoC can kick each bunch individually with low crosstalk

B. Keil et al., https://accelconf.web.cern.ch/ibic2024/pdf/WEP42.pdf

Summary

- Direct sampling @ 32 GSample/s with FPGA dot products & division measures bunch charge Q and arrival time Δt continuously, bunch by bunch and turn by turn.
- Normalizing Q·Δt by Q removes charge dependence
- Much larger linear arrival-time range compared with the 1.5 GHz analog mixer.
- Beam measurements agree with the much slower CPU-based FPFB reference, robust for large arrival time or RF phase shifts (no more LO phase tuning).
- 312ns added FPGA pipeline latency, dominated by divider for charge normalization: O.K. for SLS 2.0, could be improved (a lot …) for shorter rings.
- Logic/DSP headroom remains large. Next steps: Close the longitudinal loop with direct RFSoC DAC kicker drive, use external DRAM for larger waveforms, correct interleaving imperfections (delay, gain) by dot product coefficient tuning/calibration, …

Thank you for your attention!

Thanks to:

Pedro Baeta & David Madlener (RFSoC firmware/software development)

Karlo Lajtner (installation & PCB support)

David's Poster: WEP036 (RFSoC Gen. 3 general-purpose ADC recorder & DAC waveform generator, incl. 32 GSPS ADC stream scalar products …)

Backup Slides …

SLS 2.0 MBFB: RFSoC Logic Resources (3D MBFB Algorithm using old analog Mixing BPM RFFE & Analog Long. Kicker Upconverter)

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Post-Implementation Resource Utilization
All Planes X, Y, S on a Single Device

Resource	Utilization	Available	Utilization (%)	Utilization / Plane (%)
LUT	67597	425280	15.89	5.30
LUTRAM	4695	213600	2.2	0.73
FF	82216	850560	9.67	3.22
BRAM	449	1080	41.57	13.86
DSP	332	4272	7.77	2.59
IO	19	347	5.48	1.83
GT	1	16	6.25	2.08
BUFG	14	696	2.01	0.67
MMCM	1	8	12.5	4.17

Intentionally high to max out diagnostics RAM buffers, can be reduced

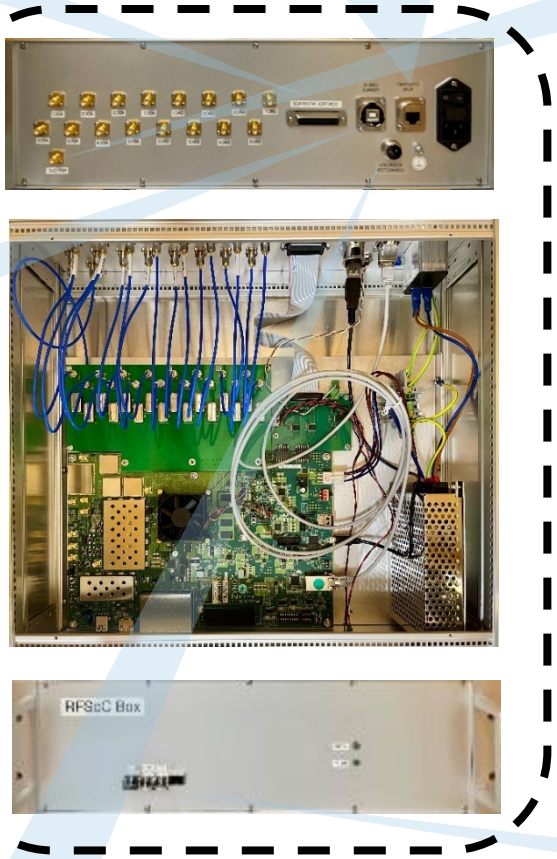
SLS 2.0 MBFB: Hardware Used for SLS 2.0 Commissioning

Serial control interface to the SLS 2.0 RFSoC RFFE

Ethernet connection to the control-system network

Machine reference clock input (f_{RF} = ~500 MHz) synchronizes data converters and programmable logic (PL)* (required modifications on the board evaluation board clocking tree)

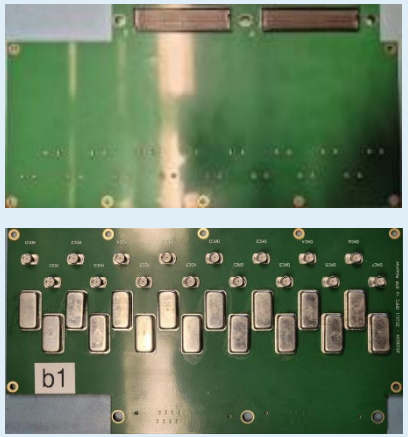
USB serial port



SLS 1.0 I-Tech analog RFFE

RFSoC Box

PSI add-on card breaks out the RFSoC ADC/DAC inputs and outputs to SMA connectors



Zynq® UltraScale+™ RFSoC Gen 1 XCZU28DR

Beam Dump Controller (BDC) interface

Gigabit fiber-optic links to the Event Master and Filling Pattern Monitor systems