Beam Position Monitor Electronics for ALS-U using RFSOC

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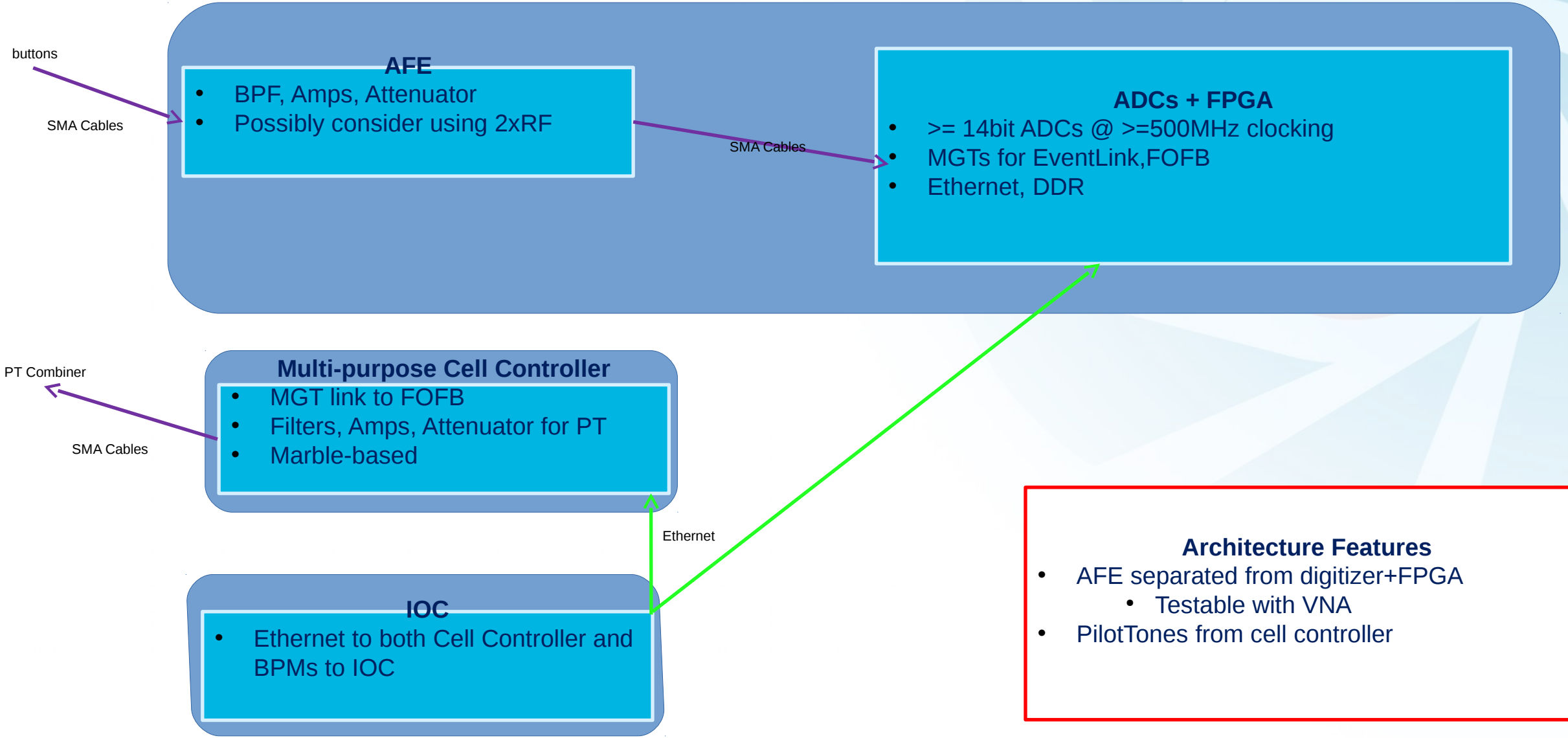
Why RFSOC was considered for ALS-U

- The original 10-year old ALS BPM system was initial candidate for ALS-U, but:
  - The BNL Digital Front End by Joe Mead works very well, but the Virtex-6 FPGA is nearly full and EOL soon (2025)
  - The LTC2208 ADCs clocking at 117MHz required two BPFs to reject images below RF
  - Sampling clock used a custom VCXO, making changes difficult
  - Pilot Tones generation using PLLs was inflexible and required a separate chassis (Cell Controller), not easily controllable from BPM
  - Single PCB for Analog Front End (BPFs, amps, DATs, ADCs) made debugging/upgrades/repairs difficult
- The ALS High Speed Digitizer by Jonah Weber and Eric Norum using Gen2 RFSOC, had worked very well: https://proceedings.jacow.org/ibic2020/papers/wepp16.pdf
  - but characterization of 12-bit ADC data didn't look promising as a BPM
- However, Gen3 was just being released, so the plan became:
  - Evaluate RFSOC as option to FPGA + ADCs
  - Modularize AFE that could accommodate either option

RFSOC Features

- 5GSPS (~3240 samples/turn) ADC eliminates alias-images for 500MHz input
  - 4 independent “tiles” of 2 channels each; two BPM button sets can be processed
- Given no images, modest BPFs will work for AFE
  - Larger BW reduces turn-blending, makes possible to resolve groups of isolated bunches
  - ALS BPM requires close-in PT of ½. RFSOC PT correlation to RF appears better, even at 2.5 bins (wider flattop of filtering)
- Direct Digital Downconversion (NCO mixer-> FIR -> Decimation) means FPGA can clock at reasonable speeds (~125-500MHz) and still have benefits of 5GSPS sampling.
  - Alternatively, ADC datastream at full-speed can be captured to Block RAM
- 4 tiles x 2 channels each of 10 GSPS DAC
  - Very powerful PilotTone generator and diagnostic tool

Early Proposed BPM Block Diagram, derived from existing ALS



Architecture Features

- AFE separated from digitizer+FPGA
  - Testable with VNA
- PilotTones from cell controller

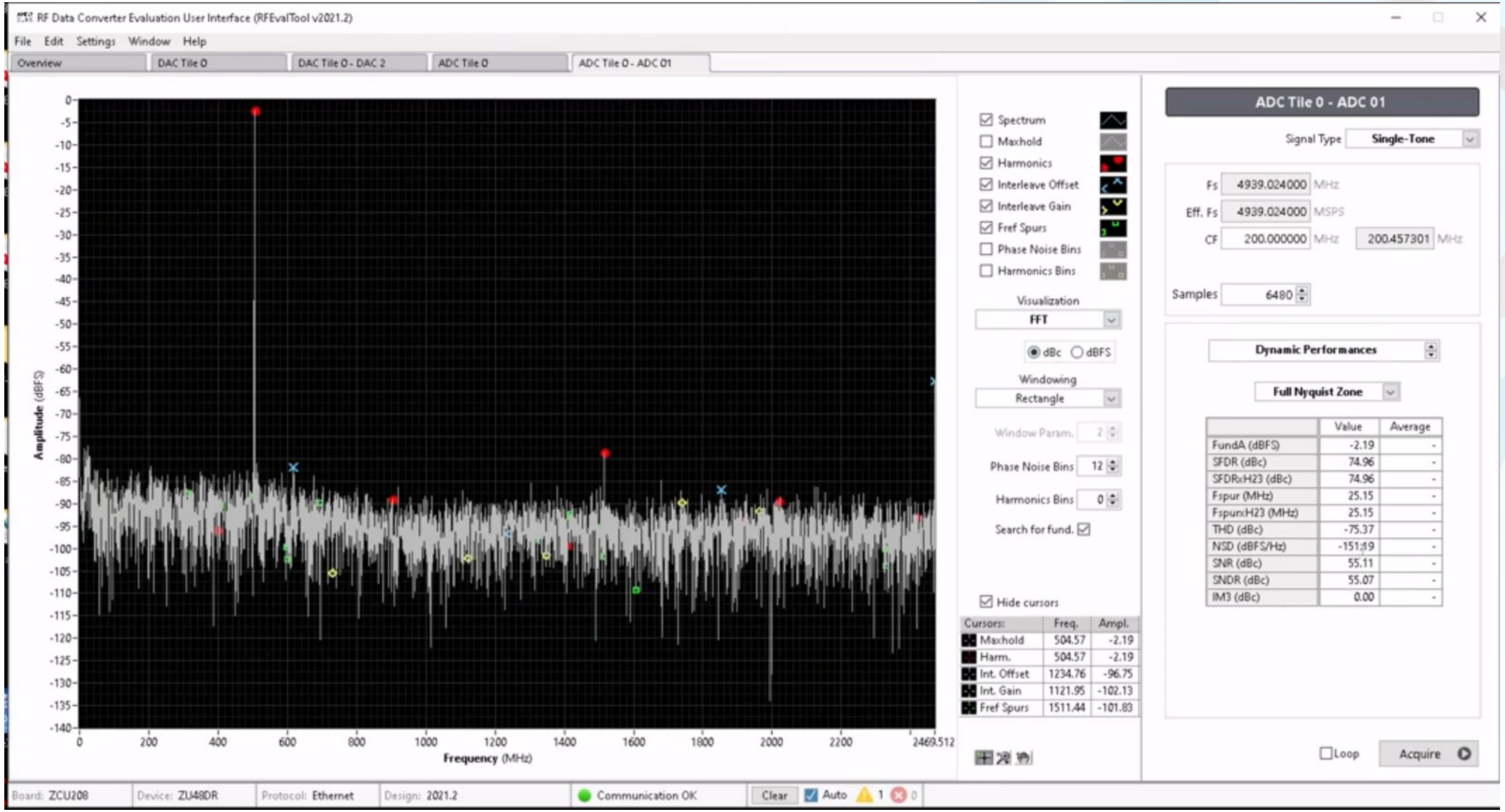
ADC Considerations

- High-performance ADCs: >= 14bits/1GSPS, sometimes with multiple channels
- These ADCs use multiple Multi-Gigabit Transceiver channels to get data into the FPGA
  - MGTs streams from multiple ADCs are tricky to synchronize
  - Difficult capturing Full Speed ADC data into FPGA
- At 500MHz input, the NSD will be <= -150dBFS/Hz, however:
  - For a ratiometric measurement, “differential” NSD is more important and is not characterized by IC manufacturers
  - Common mode effects (potentially like clock jitter) → multi-channel ADCs might have advantage

Gen 3 Investigations using ZCU208

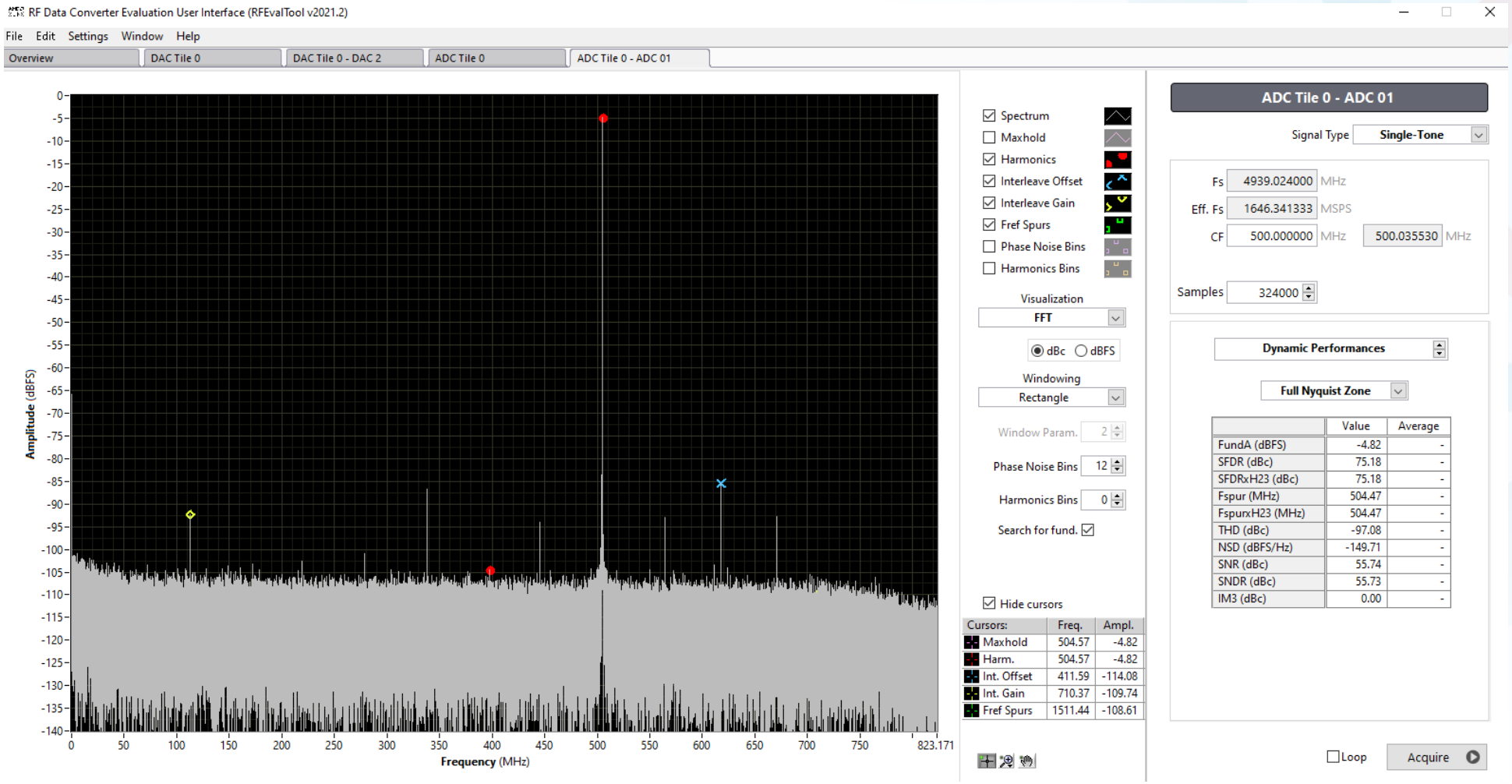
- Used ZCU208 demoboard with “Evaluation Tool” software to verify:
  - ADCs better than -150dBFS/Hz
  - Loopbacks shows > 80dB isolation
  - DDC at 40x would result in FPGA modest data rate of 123MHz
  - Easy to lock CLK104 to RF to generate ADC clocking
- Modified “RFSOC Lounge” example projects to capture all 8 ADC DDC datastreams to DDR
  - Used DACs to generate Pilot Tones
  - Uploaded waveforms for analysis, and showed TBT and SA/PT would likely meet ALS-U specs

Evaluation Tool with ZCU208 looping back DAC0 output ~500MHz CW to ADC0, showing NSD of -151dbFS/Hz



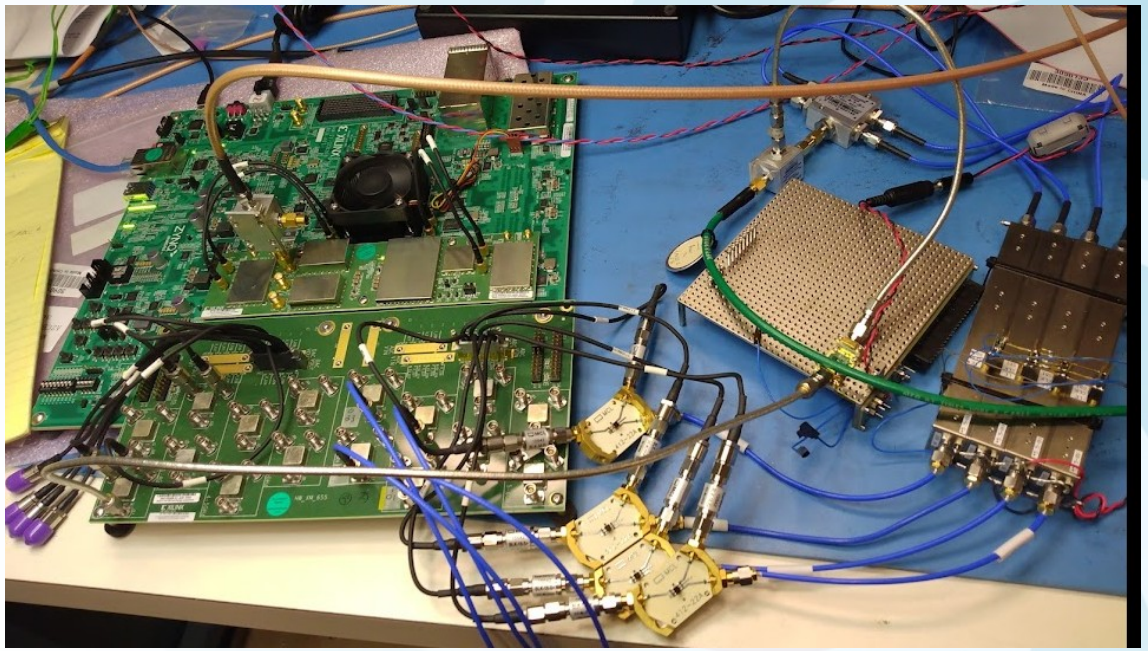
ZCU208 324K samples Capture at FADC = 1.6GSPS into DDR memory (BRAM limited to 16K samples)

- 300 turns = 200us capture length
- Decimated 3x datastream lower frequency allows DDR capture.
- Specifying no mixer is the equivalent of normal non-DDC sampling at 1/3 the 4949MHz rate (with an FIR rolloff at ~750MHz)

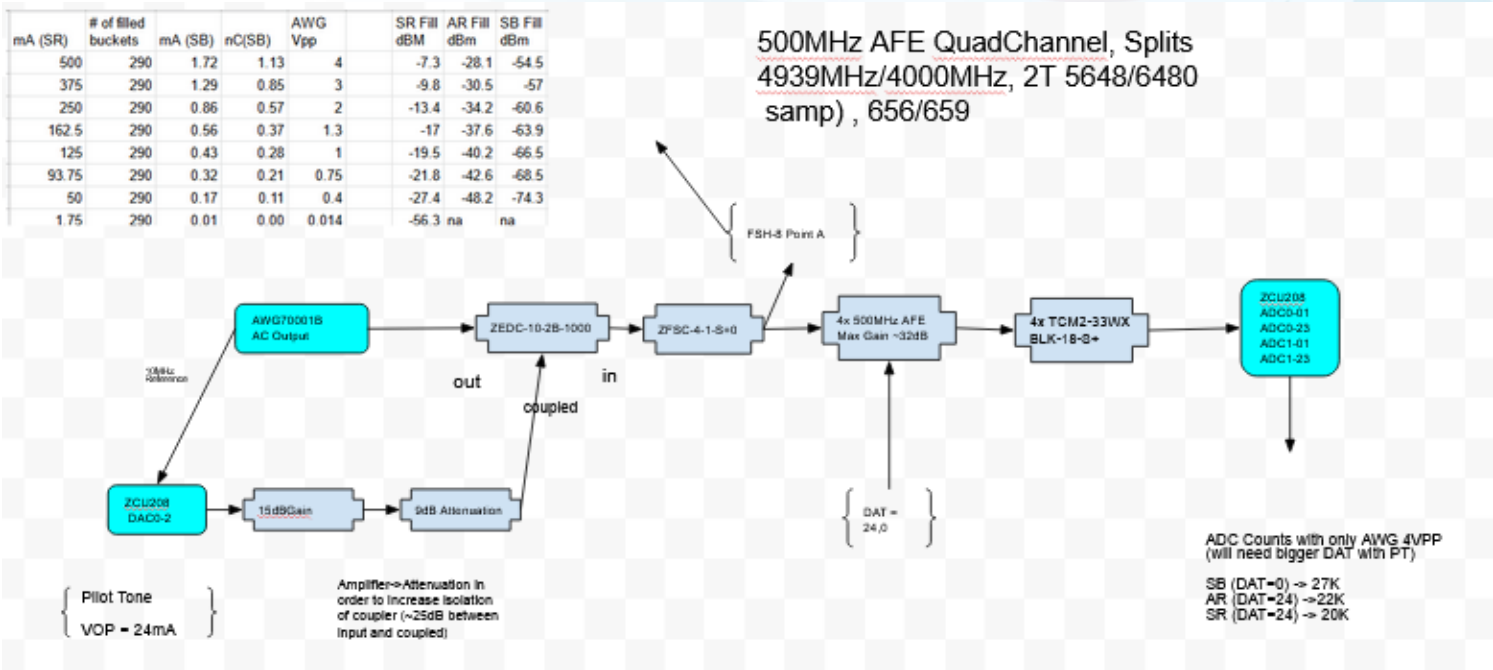


Initial Bench Test setup

- ZCU208 Xilinx RFSOC Demoboard
  - 8x 14-bit ADCs clocked at ~4939MHz.
  - Four Channels full speed data captured in Block RAM for 90K samples.
  - Digital Down Conversion rate is 40x (125MHz); all 8 IQ channels captured into 4G DDR.
  - Data is collected by PC for analysis
  - 14-bit DAC generates Pilot Tone from phase-locked 4000MHz DAC (at bin 328.5 typically)
- AWG 70001B generates 1-Turn button waveform
  - Waveform from measurement with 70GHz DPO77002SX realtime scope at ALS
  - AWG supplies 10MHz reference to lock ZCU208
  - Waveform is 50 points/2ns bucket (16400 points)
- Pilot Tone (ZCU208) and BPM signal (AWG) are combined with ZEDC 10dB coupler, with an extra amplifier & 9dB pad for isolation



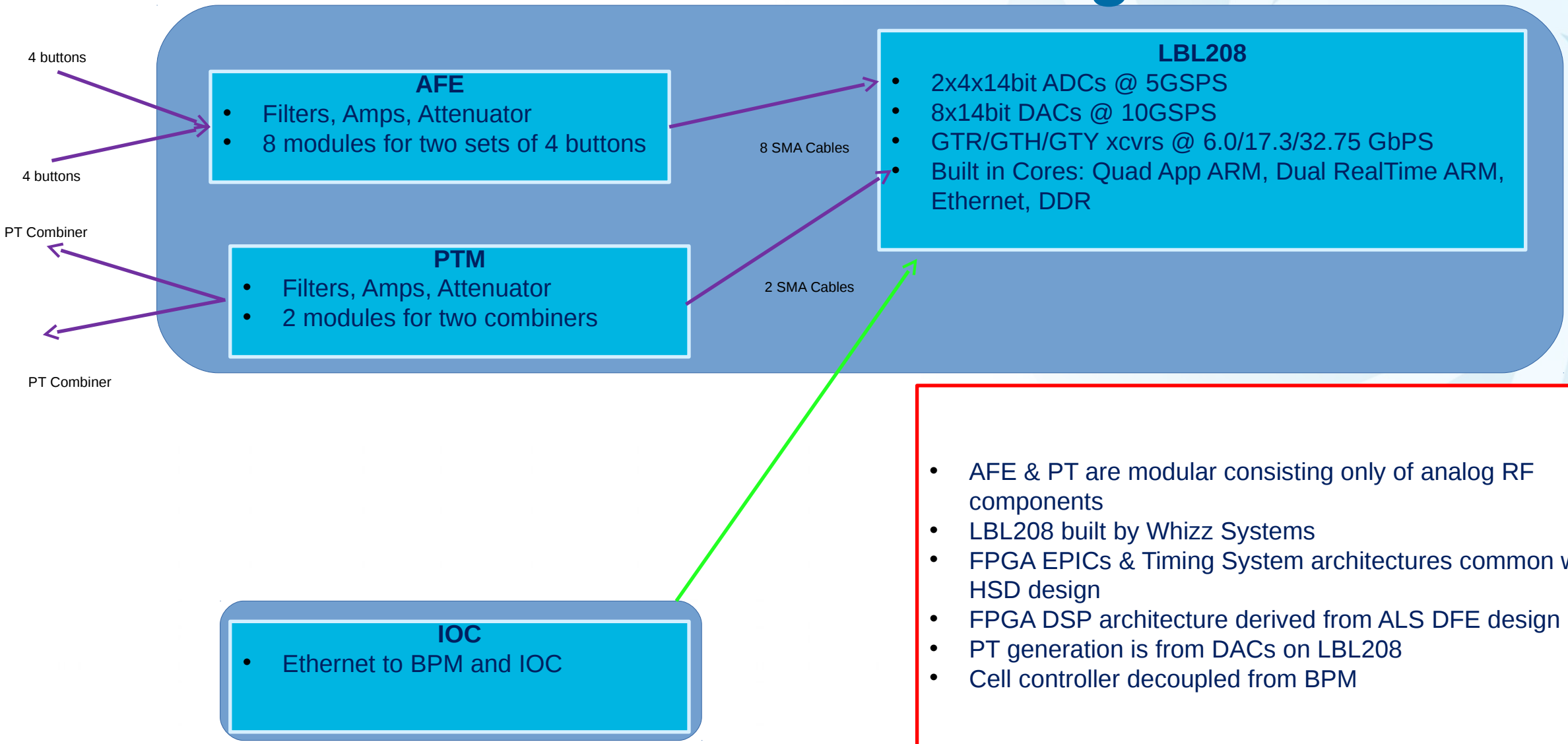
mA (SR)	# of filled buckets	mA (SB)	nC(SB)	AWG Vpp	SR Fill dBM	AR Fill dBm	SB Fill dBm
500	290	1.72	1.13	4	-7.3	-28.1	-54.5
375	290	1.29	0.85	3	-9.8	-30.5	-57
250	290	0.86	0.57	2	-13.4	-34.2	-60.6
162.5	290	0.56	0.37	1.3	-17	-37.6	-63.9
125	290	0.43	0.28	1	-19.5	-40.2	-66.5
93.75	290	0.32	0.21	0.75	-21.8	-42.6	-68.5
50	290	0.17	0.11	0.4	-27.4	-48.2	-74.3
1.75	290	0.01	0.00	0.014	-56.3	na	na



Decision: RFSOC or FPGA+ADCs

- The LBNL-designed “Marble” using a Kintex7 appeared to have enough FPGA resources to do BPM DSP, and this board has a long successful history for LLRF. However:
  - Lab testing of the proposed in-house ADC board indicated that it would need rework to evaluate 500MHz direct sampling
  - ADC board clocking would need to be reworked to use MRF as reference
- RFSOC would likely meet specs, and promised high levels of system integration. However:
  - Use of a ZCU208 in production?
  - The RFSOC chips are several months lead-time and costly
- ALS-U decides to continue RFSOC effort
  - L. Russo commences gateware and PS platform design on ZCU208.
    - https://proceedings.jacow.org/icalepcs2023/papers/thpdp080.pdf and in MORT07 of IBIC2026
    - Not clear if gateware design for XCZU48 will cleanly port to XCZU47…
  - Need to figure out how to get an RFSOC PCB built
  - Need to control costs
    - John Joseph (ALS-U Instrumentation CAM) initiates discussion with Avnet:
      - LBNL research, including imaging the Covid virus at ALS, during pandemic
      - RFSOC technology might be an important tool for this research
    - Avnet generosity keeps the RFSOC effort alive

ALS-U BPM Block Diagram



- AFE & PT are modular consisting only of analog RF components
- LBL208 built by Whizz Systems
- FPGA EPICs & Timing System architectures common with HSD design
- FPGA DSP architecture derived from ALS DFE design
- PT generation is from DACs on LBL208
- Cell controller decoupled from BPM

Getting an RFSOC PCB: Evaluate two vendors

- In order to make the chip costs feasible, all 8 ADCs would be deployed (2 button sets)
  - This requires that the isolation between button-sets be about 80dB (the worst case would be a button set that gets taken out during operation).
  - LBL208 crosstalk described : https://arxiv.org/pdf/2510.13192
- The Avnet-XRF8 provided a SOM, had a nice mechanical/thermal design. It was also very compact compared to the ZCU208. However testing revealed:
  - The isolation was about 10dB worse than ZCU208
  - The designer confirmed the measurement, speculated it was because of the compactness of the layout.
  - Cost
- The RealDigital 4x2 was just released, Good usability from PYNQ. However:
  - Possibly because of compact design, isolation was about 10dB worse than ZCU208.
  - Would have required negotiating a custom redesign since it only has 4 ADC channels implemented.

Decision: Engaging a design/fab house

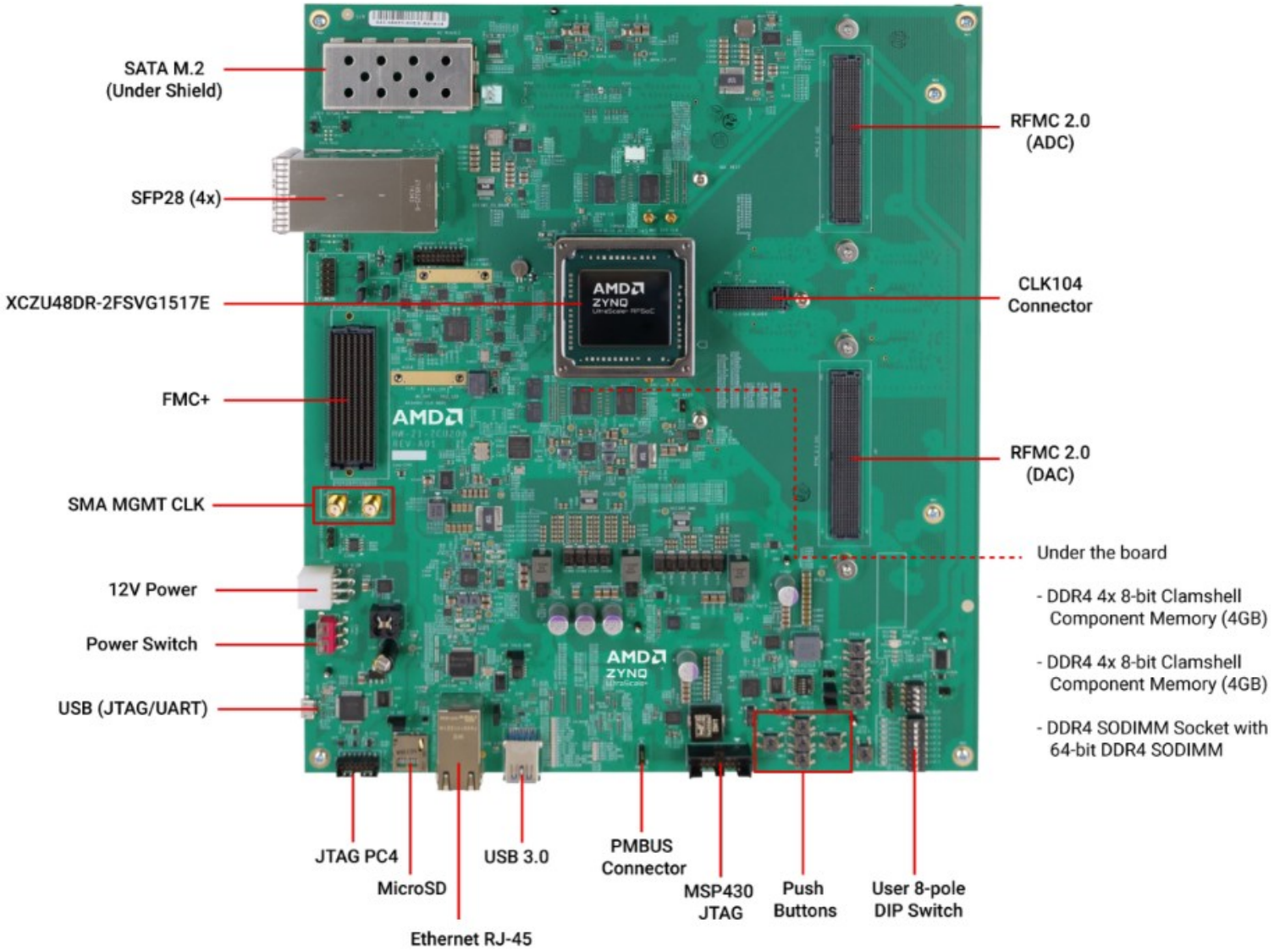
- Notice sticker on ZCU208 referencing “Whizzsystems”.
  - https://www.whizzsystems.com/about#sec2
  - Whizz has built recent Xilinx demoboards: RFSOC (ZCU111, ZCU208, ZCU216, ZCU670), Versal High Performance SOC (VCK190, VMK180, VPK120, VPK180)
  - They build about 700 ZCU208’s yearly
  - Santa Clara is about 1hr drive from LBNL. Begin in-person meetings to discuss a custom build RFSOC
- Entered a contract with Whizz for an “LBL208” derivative design and quantity 145 build:
  - Modification of Orcad schematic and Allegro layout to update obsolete components and move connectors for better front panel access.
  - 5 year component management
  - Turn-key manufacturing with LBL providing the FPGA
  - Unit Testing

Whizz Experience

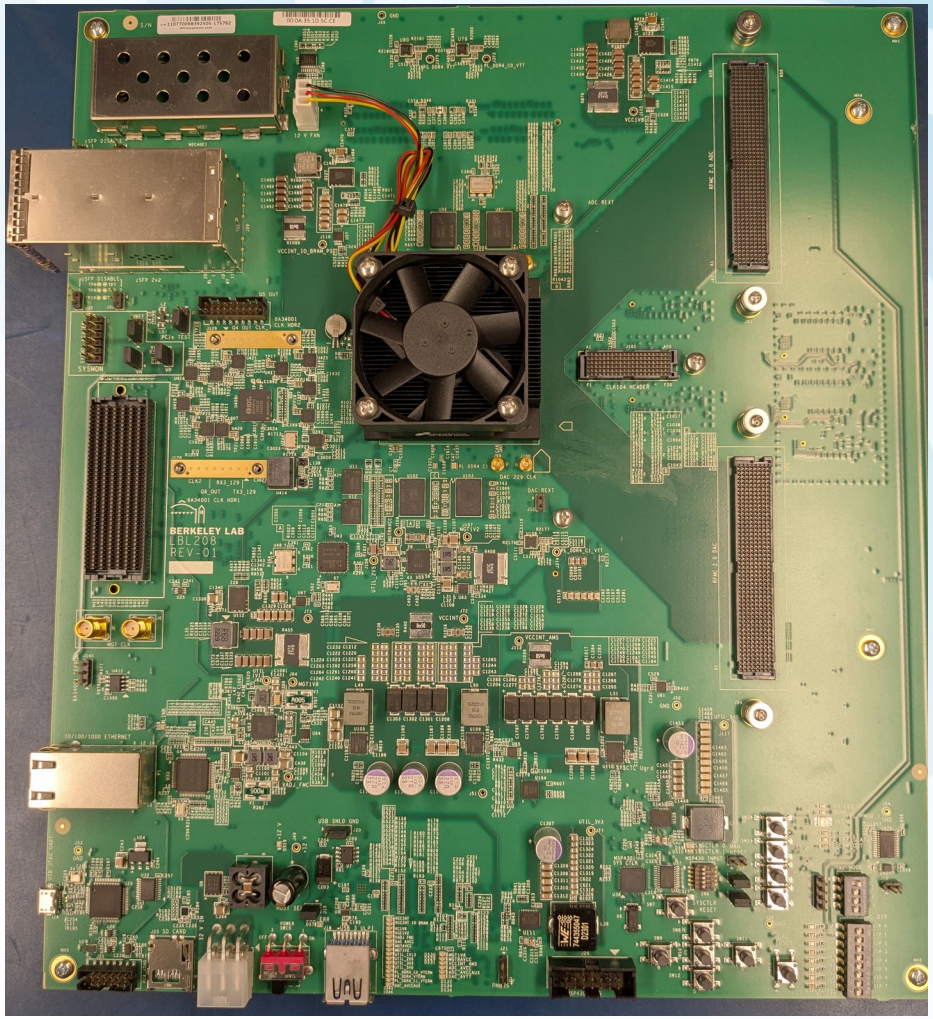
- Build #1: 5 units for first article verification tests
  - ZCU208 gateware targeted for XCZU48DR is rebuilt to target XCZU47DR
  - Bring up ported gateware on LBL208, it works!
  - All 5 boards run new BPM firmware, perform to spec

- Build #2: 70 units built
  - Whizz reports 18 units fail powerup testing
  - Extended debugging at Whizz and LBNL. Conclude it was bad lot of a power converter IC. Same chip used on ZCU208 & ZCU216 builds, but from a different lot purchased solely for LBNL.
  - 8 hour elevated temperature burnin at Whizz on remaining boards; all pass.
- Give Whizz goahead for final build #3: 70 units :
  - 2 boards fail (expected yield, given ZCU208 build history)

ZCU208



LBL208



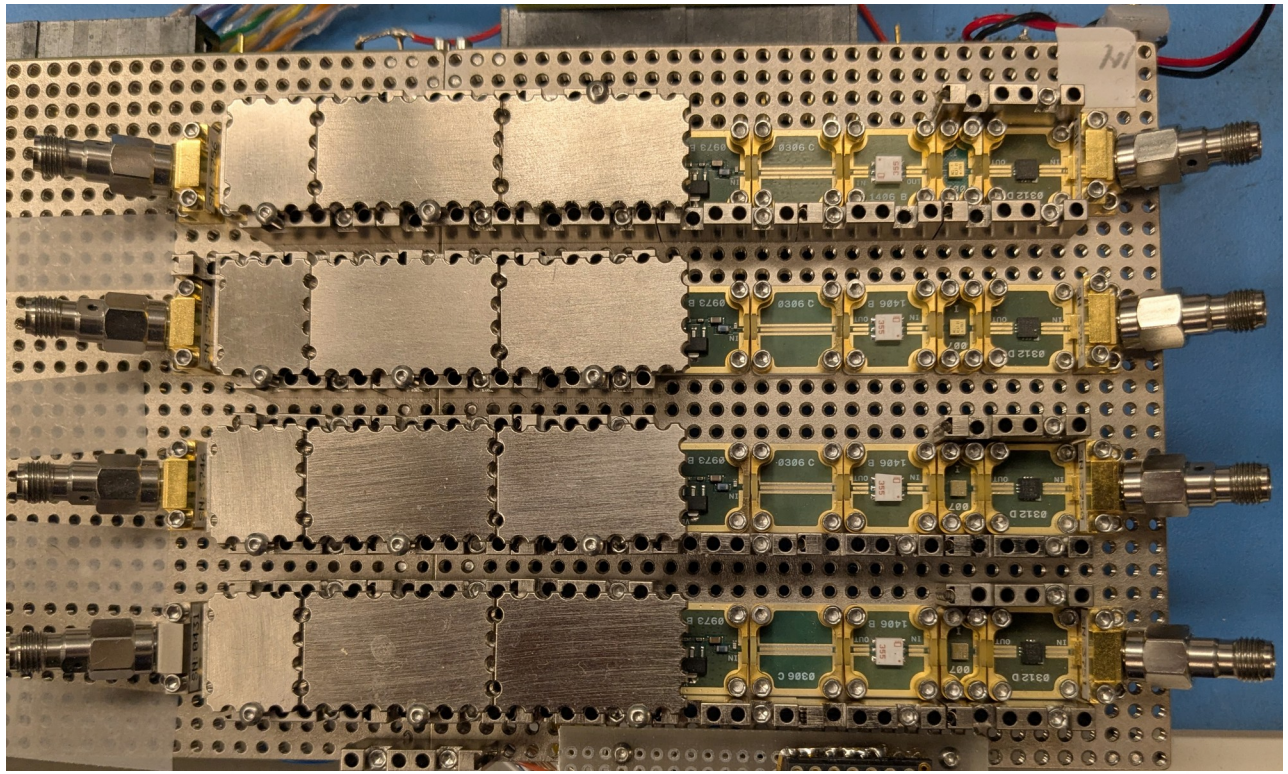
AFE Prototyping

- Used Xmicrowave prototyping system
  - “Drop-in” modules interconnected by “Ground-System-Ground”, fastened to a grid of 1-72 holes “on the grid”
  - Drop-ins from Analog Devices, Minicircuits, Peregrine (manufactures of the parts used on the ALS BPM AFE)
  - Typically a 4 layer Rogers 4003 PCB. Xmicrowave designed & fabbed a drop-in with our custom BPF
  - https://xmicrowave.com/documentation/faq/

- We build a full 4-channel AFE with drop-ins on a protoplate, used for LBL208 evaluation

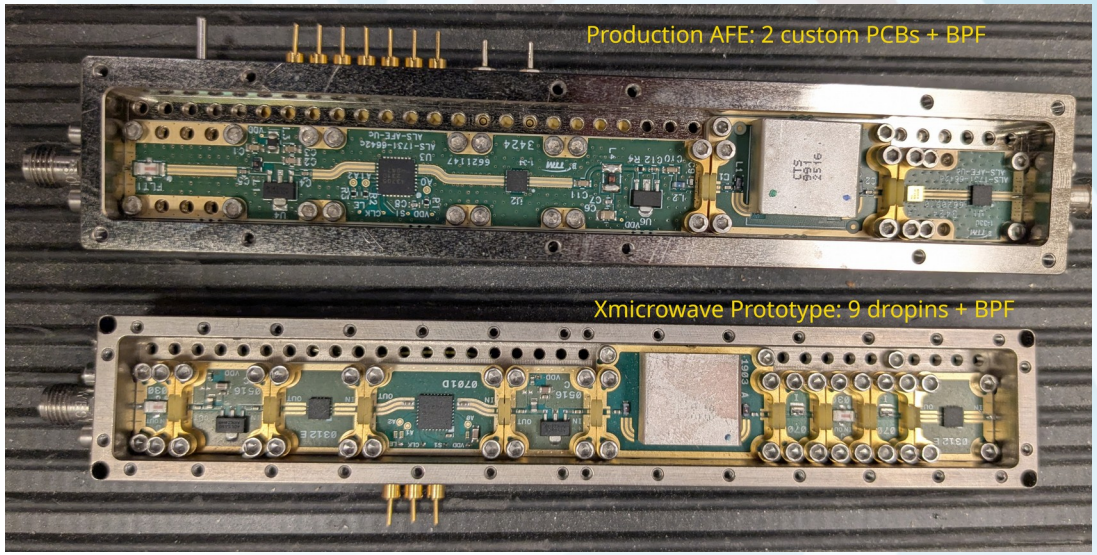
- Had Xmicrowave build 4 “Custom Microwave Assemblies” (CMA), they work well. Would have liked Xmicrowave to build production AFEs but:
  - A quote to build ~1000 AFE modules was 2x project baseline
  - Decide to build AFE inhouse, based on a module per channel like the CMA

Protoplate AFEx4



As shown, the BPFs installed are BFTC-500+, which have a 200MHz BW at 500MHz CF. These are being evaluated for measurements within a turn, like injected train behavior.

Production & Prototype



Top module is 3-board RF lineup. On bottom side of grid is a single “backside” PCB providing power and SPI control access.

Bottom module is prototype from Xmicrowave, from which the top is derived.

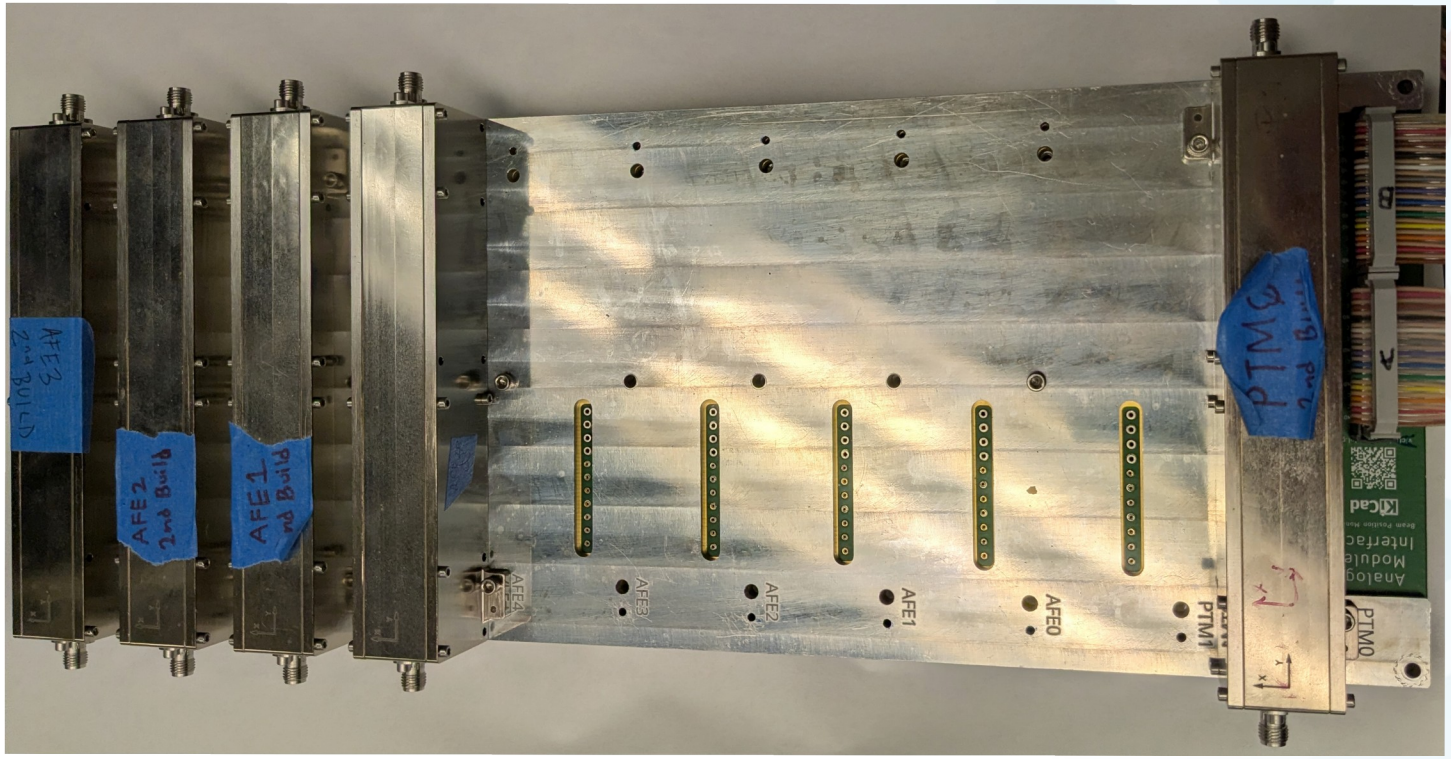
Decision: single-board vs. dropins

- Dropin (3 PCB on topside RF, 1 PCB on backside for power/SPI/monitoring)
  - (+) Easy BPF and lineup replacement, good thermal dissipation since boards are 1-sided
  - (-) 4 separate PCBs, more assembly effort

- single-board
  - (+) 1 PCB, likely easier to assemble
  - (-) hard to update. Harder thermally if 2-sided board.

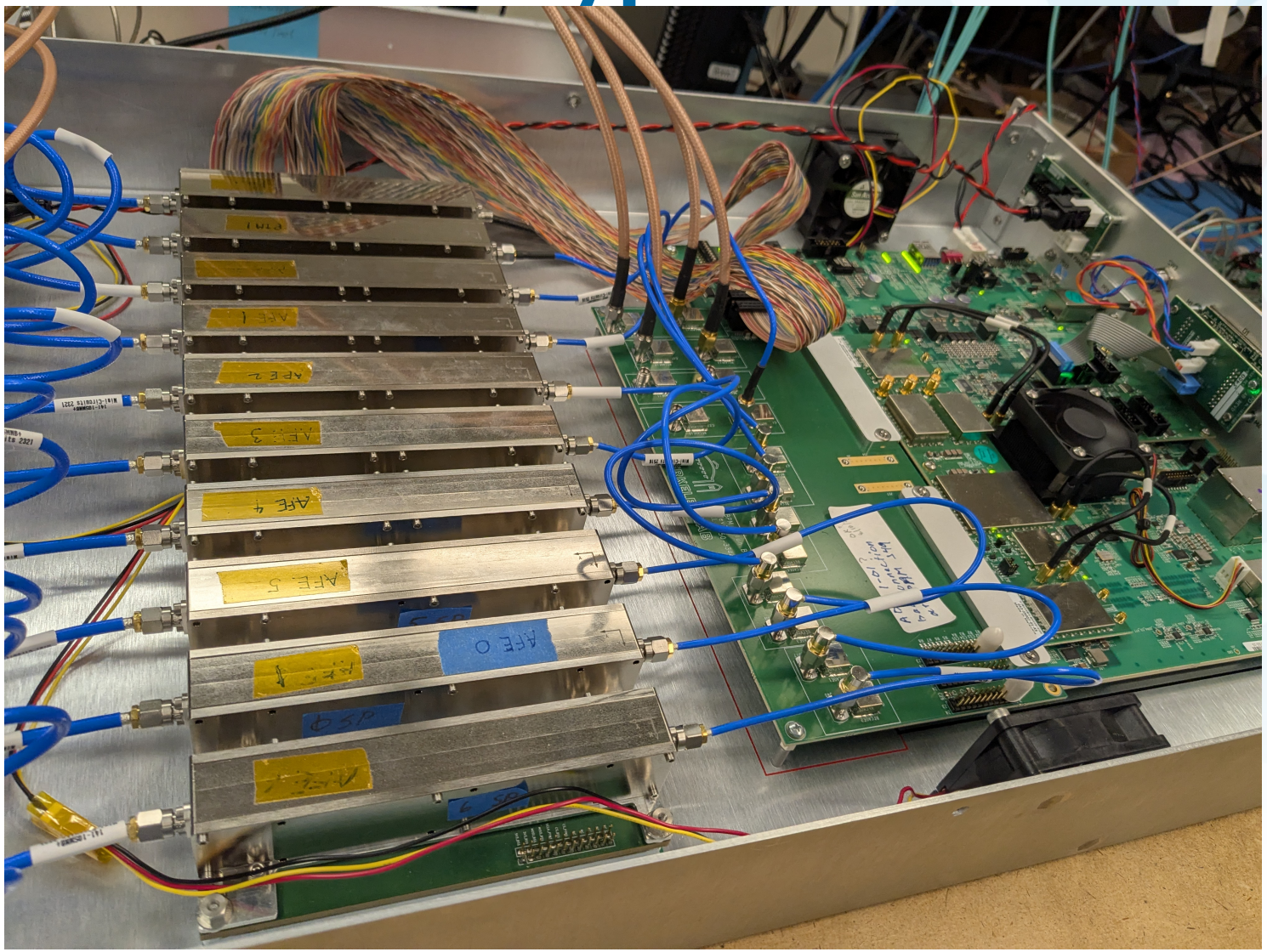
- Chose to go with dropin
  - The 4 boards did add more effort, for both PCB and enclosure design.

Analog Module Interface (AMI) with 4 AFEs and 1 PTM

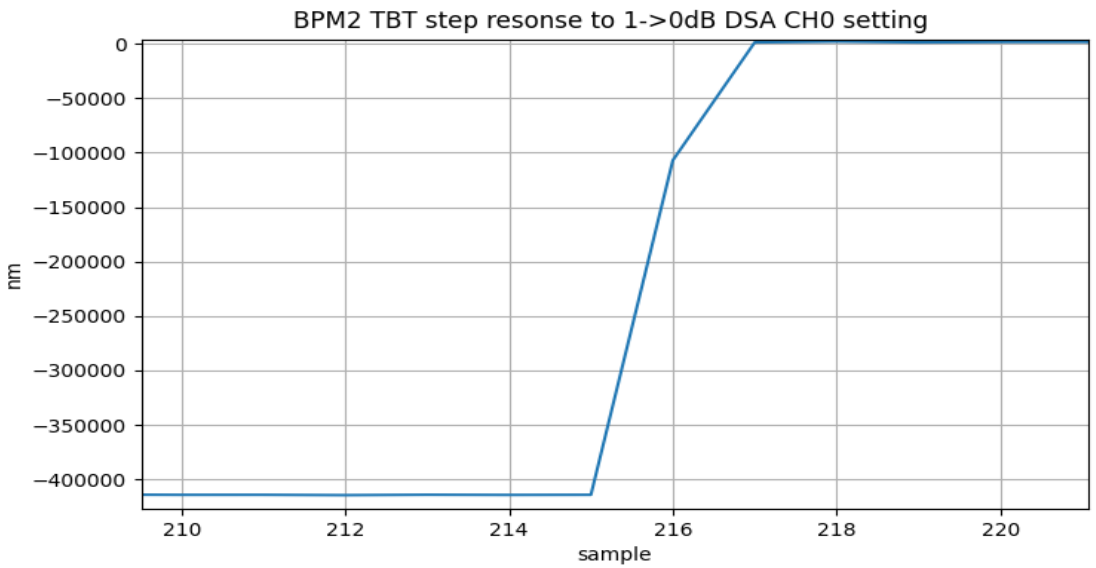


AMI is a sandwich of 1) aluminum lid, 2) PCB, and 3) aluminum baseplate. The PCB has abundant thru-hole vias for heat conduction. The AFEs and PTMs feedthru-capacitor leads plug into cage receptacles on the PCB

Prototype Chassis

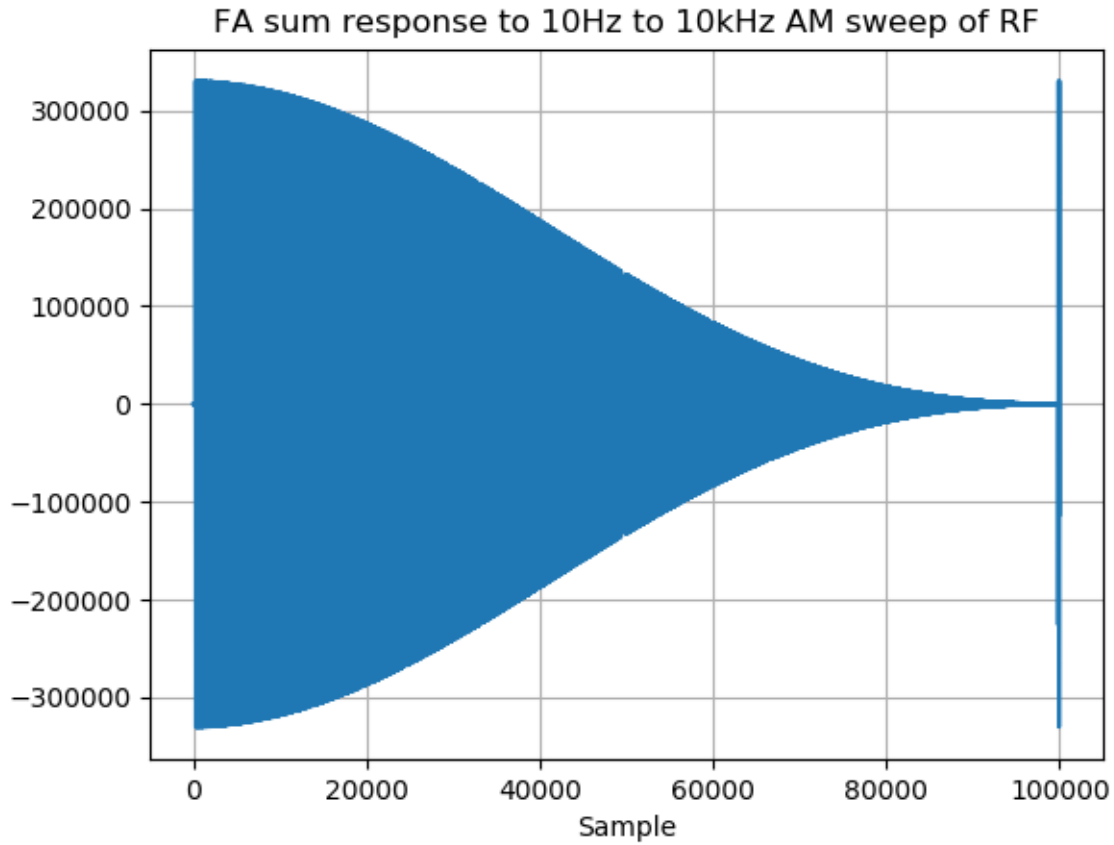


Turn-By-Turn Step



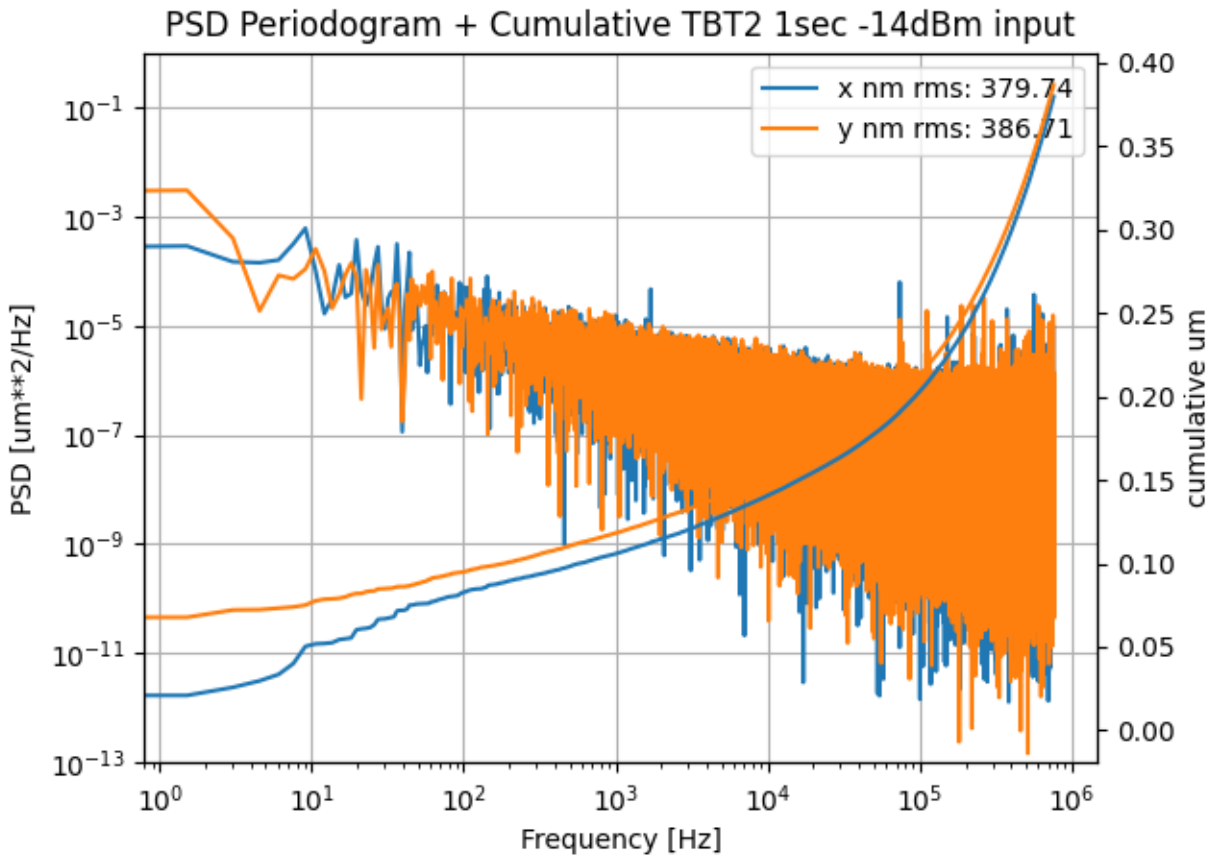
The TBT plot shows that the positional response to simulating a RF step amplitude change in ADC0-01 channel by doing a 1 sec waveform capture while the DSA goes from 1dB to 0dB. The time for the response is 2 samples.

FA 10 Second FM Sweep



The FA plot shows 10 second capture of a RF that was FM swept 10Hz to 10kHz over 10 seconds. The 3dB bandwidth is about 3kHz

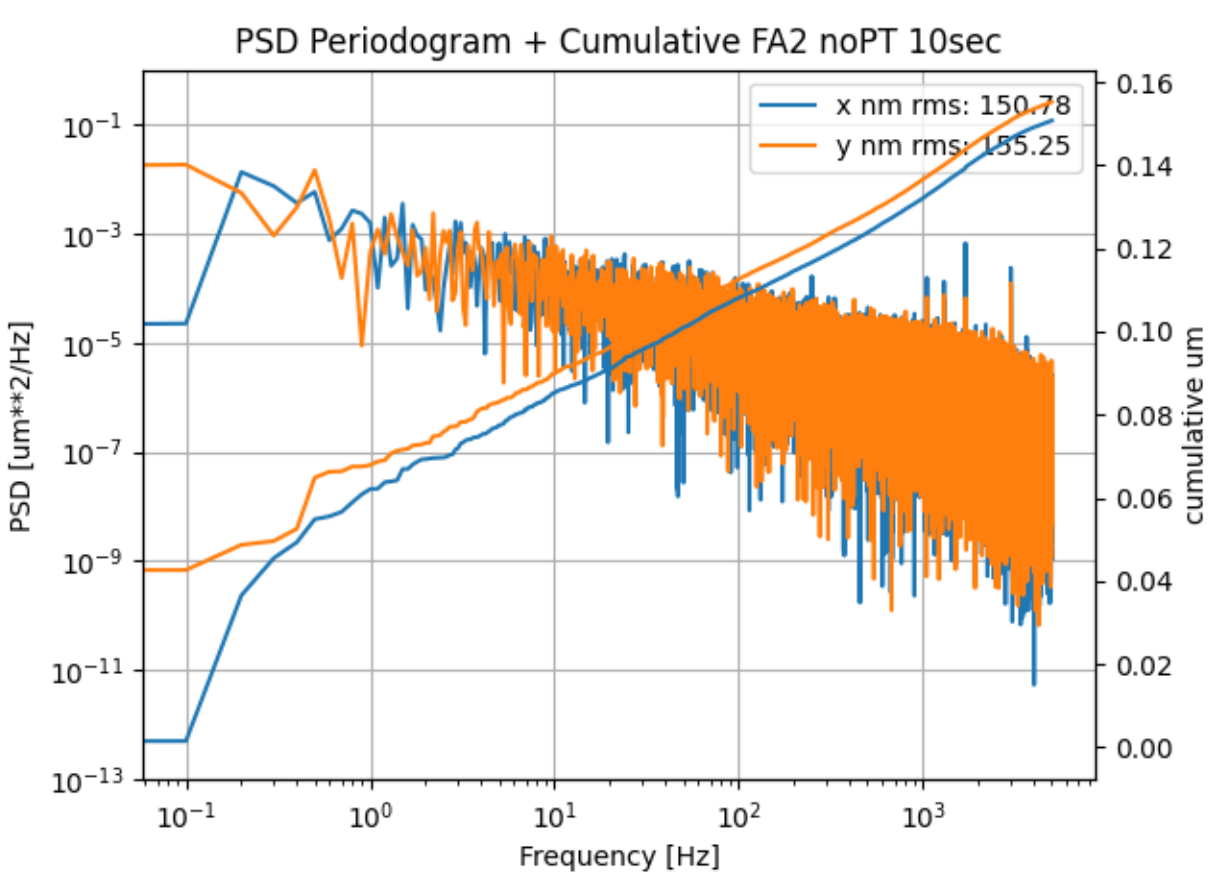
Turn-by-Turn PilotTone Off, -14dBm



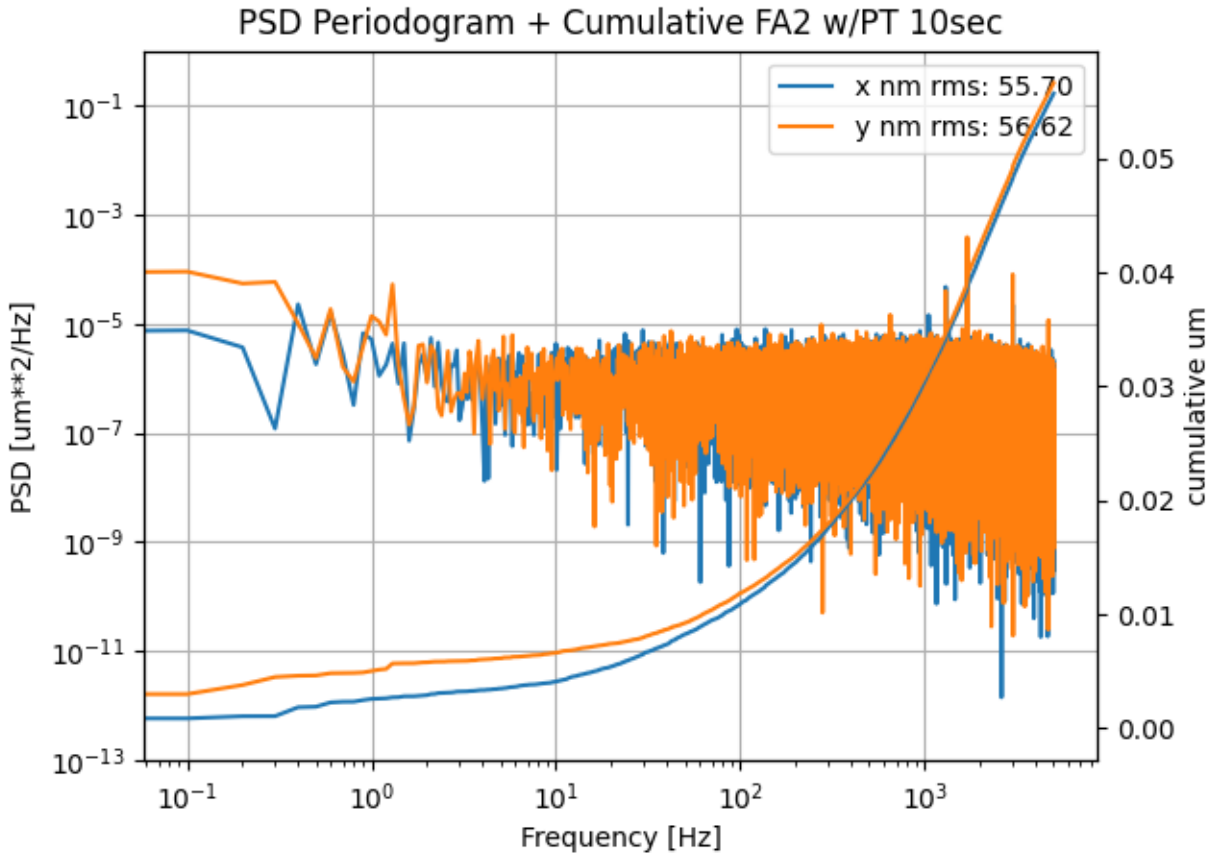
The TBT Periodograms shows total RMS noise is about 380nm.

1 second measurement, K = 16mm.

Fast Acquisition PilotTone off



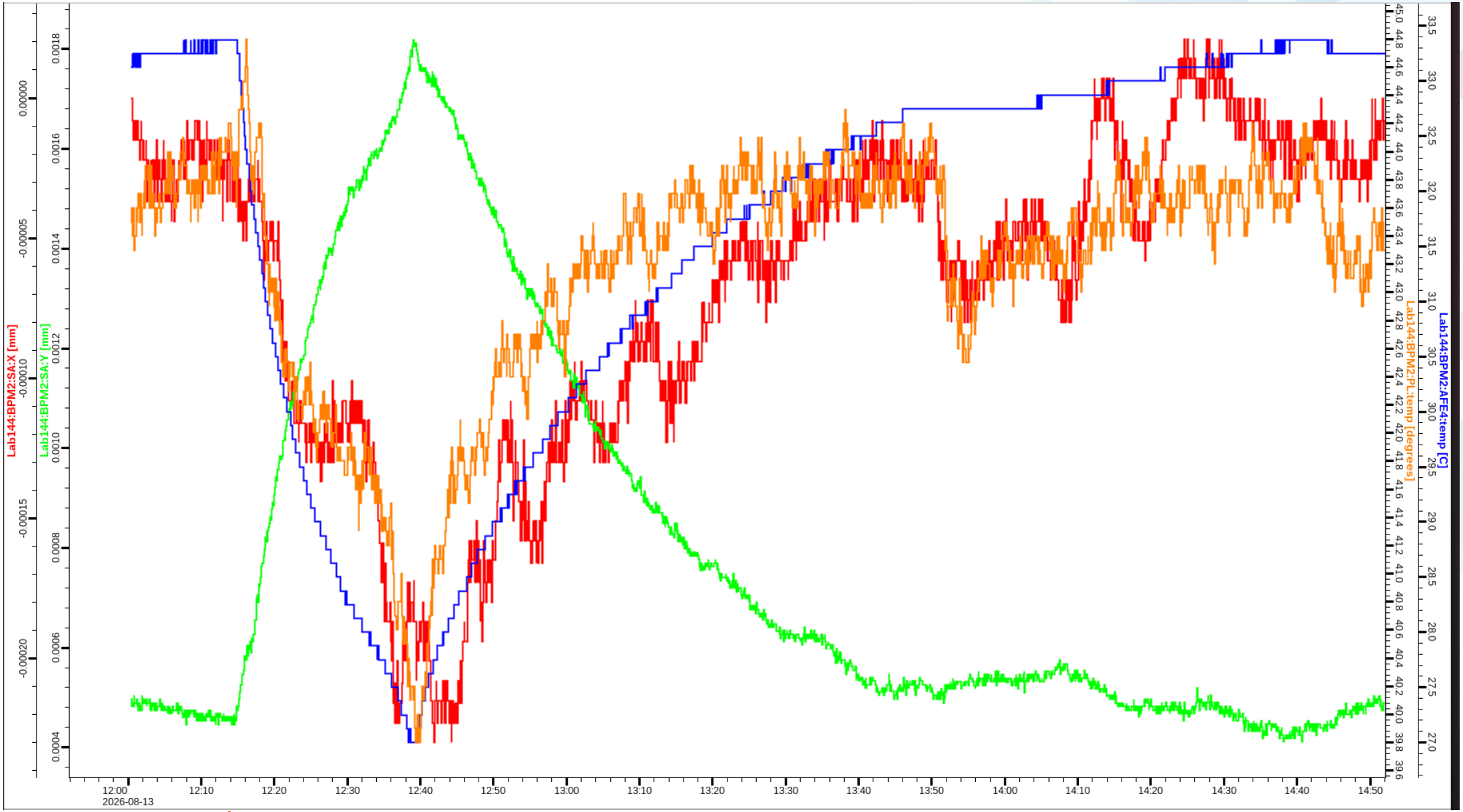
Fast Acquisition PilotTone On



The Fast Acquisition Periodograms shows that Pilot Tone reduces the total RMS noise from about 150nm to about 55nm.

10 second measurement, K = 16mm.

Slow Acquisition Temperature Response with PilotTone On



A table fan blew on the open chassis from 12:10 to about 12:40, and then it was turned off to allow the chassis to recover to normal temperature.

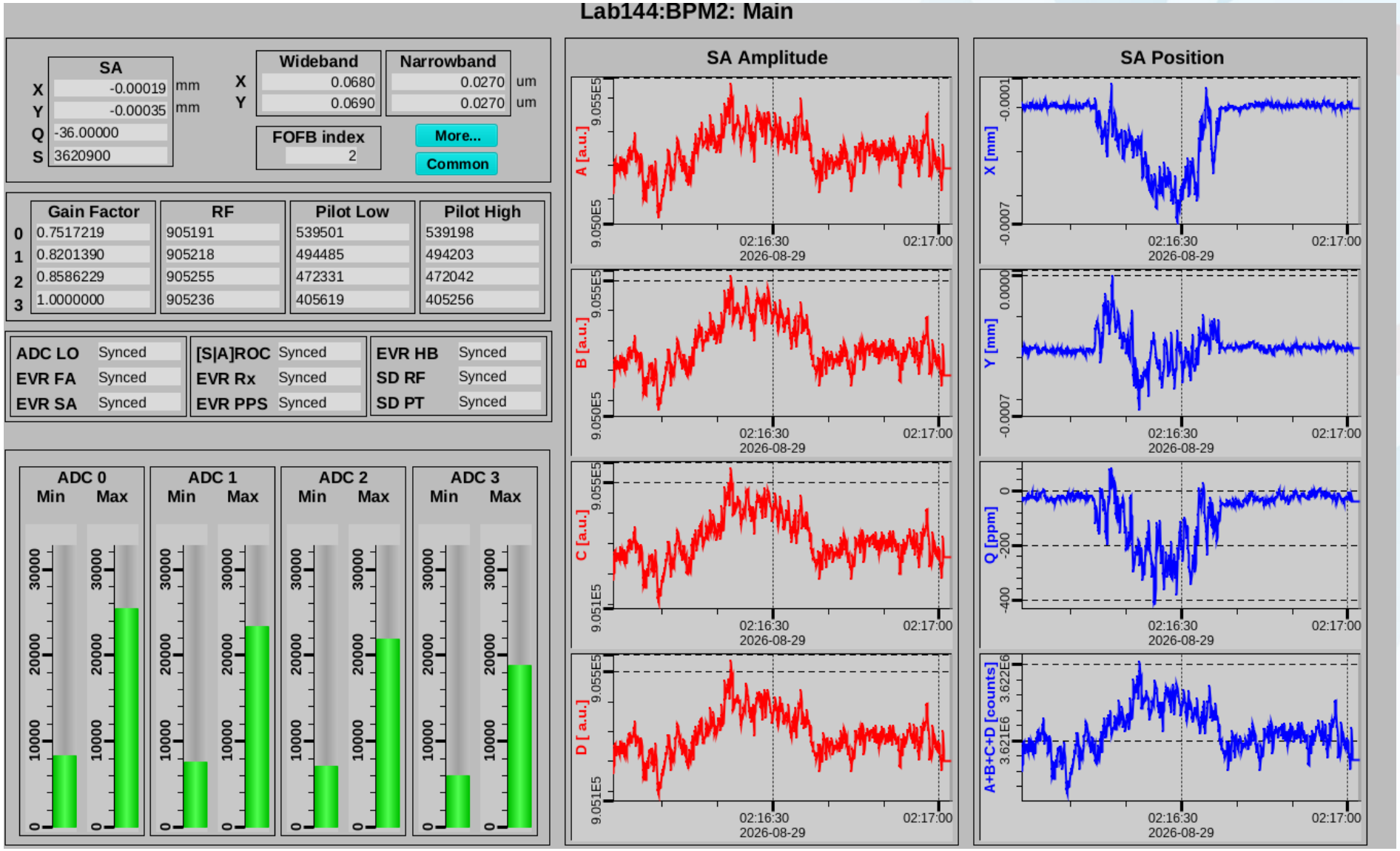
The orange trace was PL temperature from the XCZU47, and had about 5 degC span. The blue trace was an AFE module temperature and went about 6degC.

The green trace was “Y” axis position, and moved about 1.5um
“X” axis in red moved about 0.2um.

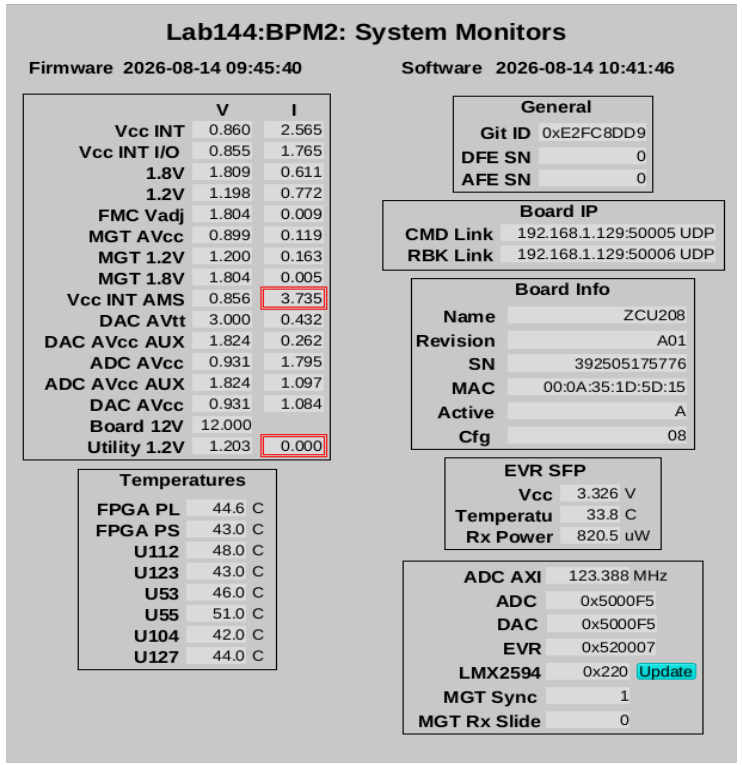
Thanks to:

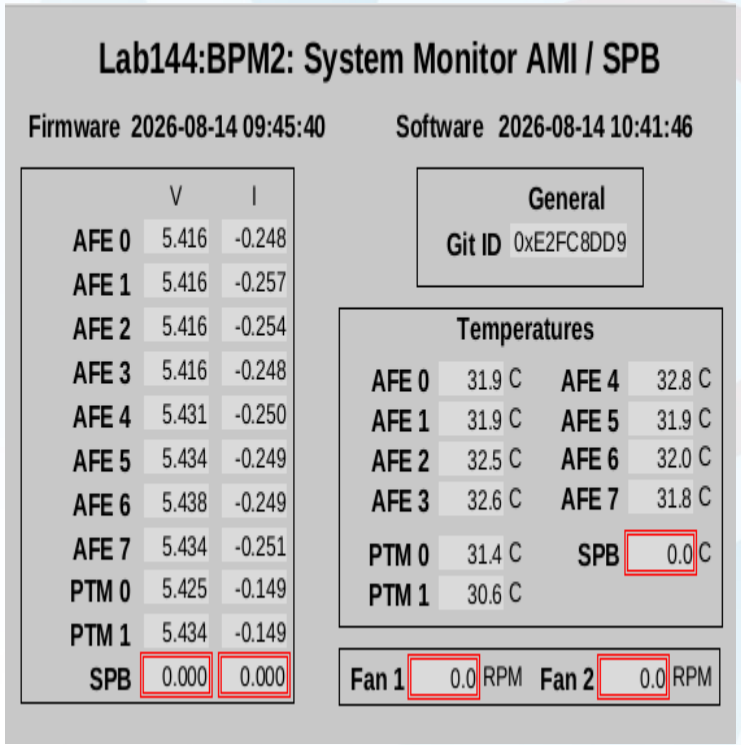
Lucas Russo	Gateware EPICS interfacing Algorithms
Nathen Ly	PTM Various Support PCBs
Victoria Moore	AMI
Jonah Weber	Front Panel Display Project Management
Changchun Sun, John Joseph	CAM
Neil Dey Kyle Gee Carol Baumann	Coordination, Mechanical Design, Procurement, Testing
Shree Murthy	First user & mentor of EvalTool
Greg Portmann	BPM Enthusiast Explainer of beam stability

Appendix-Phoebus Engineering Display PilotTones OnOffOn

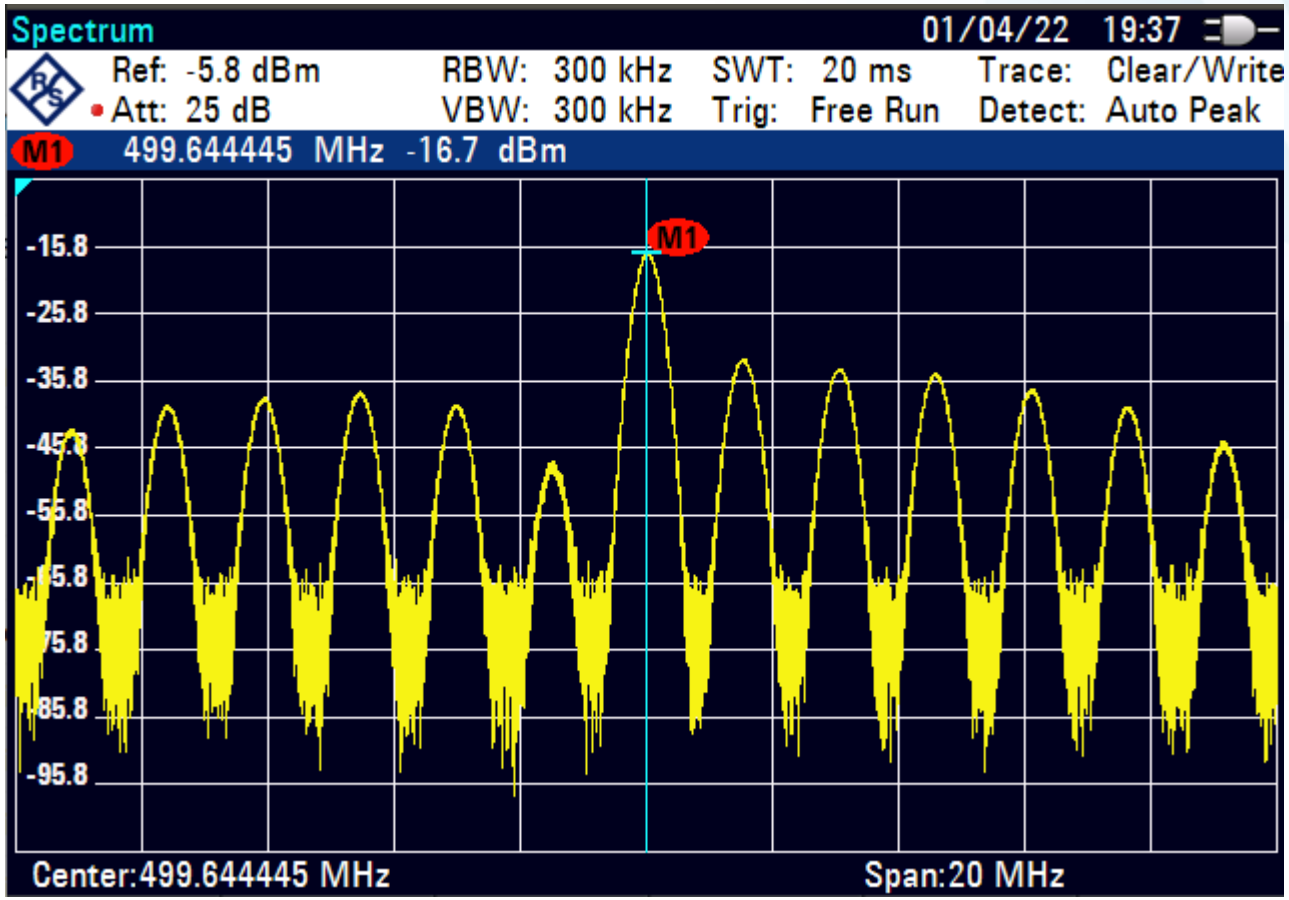


Appendix-Phoebus Sysmon

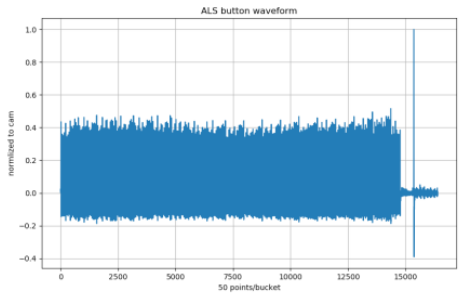


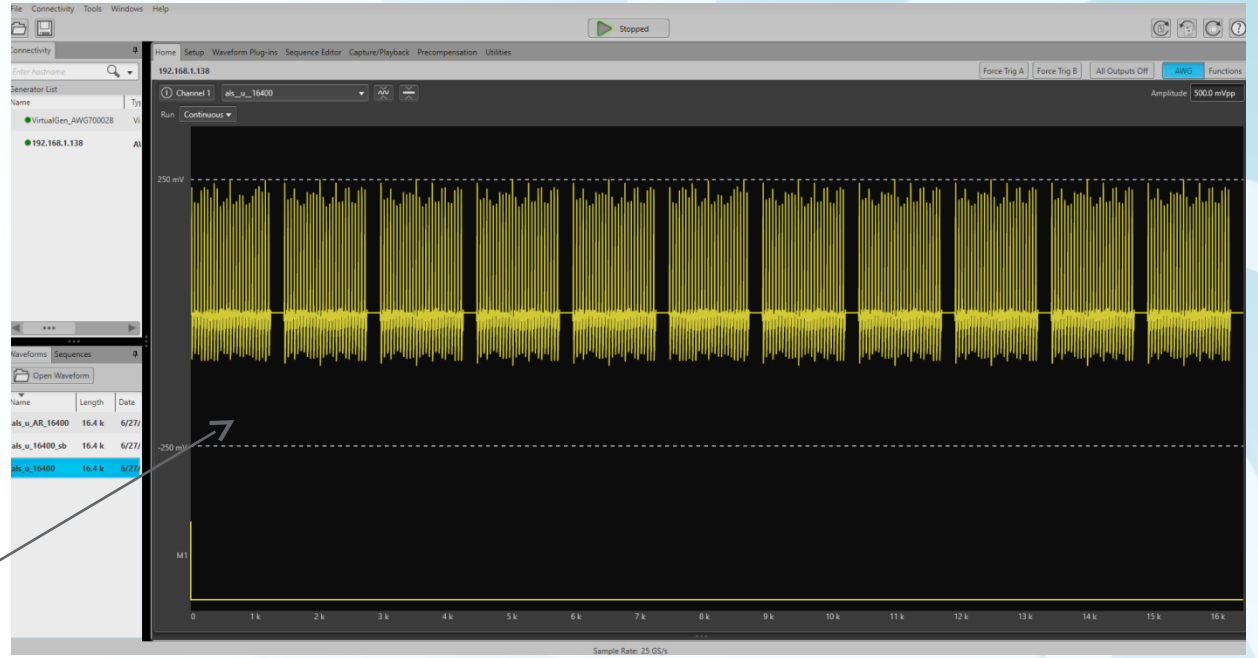


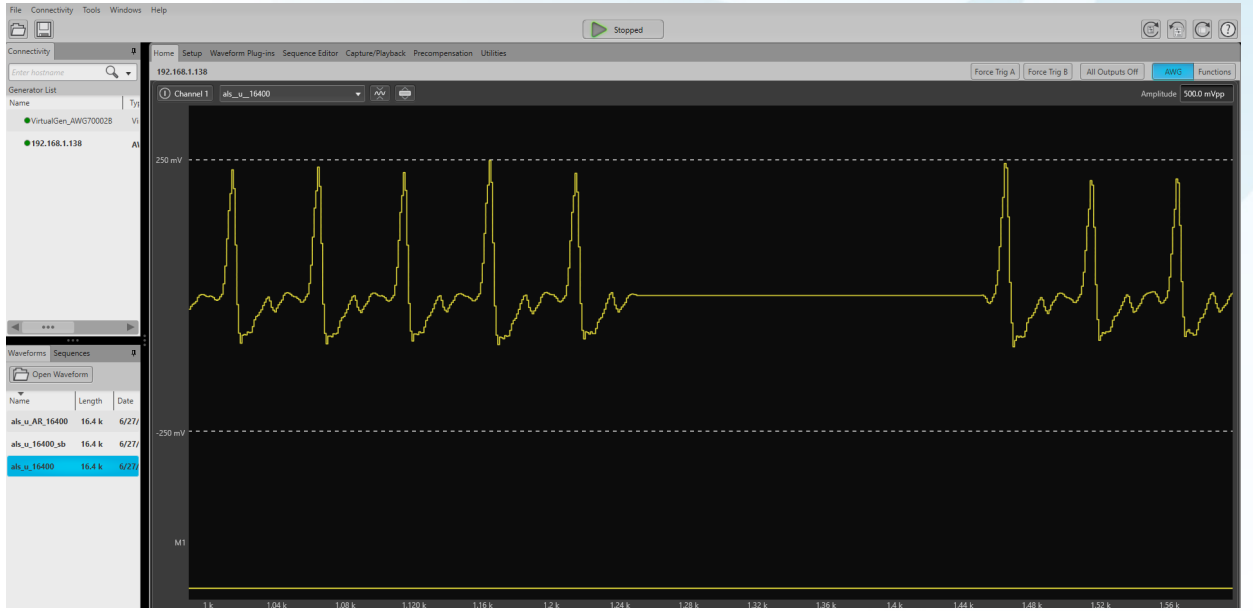
Appendix: Power Measurement of AR“Reference” button at ALS, 500mA fill. 10dB pad, so actual button power was -7dBm.



Appendix: Using ALS measurement to simulate ALS-U fill pattern







- Measurement with 70GHz DPO77002SX realtime scope at ALS showing typical user op fill (1 gap with cam bucket)
- Using python to manipulate the data in the above measurement
  - 26 or 25 filled buckets in main ALS train, added 4 empty buckets to generate 1 ALS-U train
  - 11 trains created to form the ALS-U SR fill
- 25GHz sampling speed gives 50 point per bucket; 16400 total points representing 1-Turn
- For SR waveform generation, AWG70001B output level set to 3Vpp or 4Vpp so that there is -10 or -7 dBm in the 500MHz line as measured by FSH-8 Spectrum Analyzer at the output of the 4-way splitter
- Waveform is continuously played back to simulate circulating beam

Appendix: ALS-U Button Types

	A	B	C	D	E	F	G	H	I	J	K	L
1												
2	BPM type	Original Transfer Impedance (mΩ)	Transfer Impedance (mΩ) with recession	Horiz. Sensitivity (%/mm)	Vert. Sensitivity (%/mm)	full fill current in mA (280 bunches)	Calculated button voltage	Calculated button power dBm	cable atten	Calculated rack signal dBm full fill	Calculated rack signal dBm 26-bunch	Calculated rack signal dBm single bunch
3	A1	233	233	20.1	20.1	500	0.233	0.35742	-6	-5.64258	-26.28628	-54.58574
4	A2	212	212	15.4	15.4	500	0.212	-0.46298	-6	-6.46298	-27.10668	-55.40614
5	A3	164	164	21	20.7	500	0.164	-2.69282	-6	-8.69282	-29.33652	-57.63598
6												
7	E1	106	106	29.6	7.3	500	0.106	-6.48358	-6	-12.48358	-33.12728	-61.42674
8	E2 (note 2)	113	113	26.5	12.2	500	0.113	-5.92813	-6	-11.92813	-32.57182	-60.87129
9												
10			0									
11	K1	171	171	17.4	22.6	500	0.171	-2.32978	-6	-8.32978	-28.97347	-57.27294
12	K2	172	172	17.6	23.2	500	0.172	-2.27913	-6	-8.27913	-28.92282	-57.22229
13												
14	F1	219	219	15.4	15.3	500	0.219	-0.18082	-6	-6.18082	-26.82451	-55.12398
15	F2	235	235	15.3	15	500	0.235	0.43166	-6	-5.56834	-26.21204	-54.51150
16	F3	162	162	21.4	20.5	500	0.162	-2.79940	-6	-8.79940	-29.44309	-57.74256
17												
18	J1	53	53	12.1	15.8	500	0.053	-12.50418	-6	-18.50418	-39.14788	-67.44734
19												
20	L1	158	158	19.5	22.2	500	0.158	-3.01656	-6	-9.01656	-29.66025	-57.95972
21												
22	Default Sensi	6.25	6.25									
23	Recession	1										
24												